Large-Size AlGaN/GaN HEMT Large-Signal Electrothermal Characterization and Modeling for Wireless Digital Communications

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This work has been accepted by the faculty of Electrical Engineering and Computer Science of the University of Kassel as a thesis for acquiring the academic degree of Doktor der Ingenieurwissenschaften (Dr.-Ing.).

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Defense day: 22\textsuperscript{nd} November 2011
This thesis is dedicated to:

my wife, my daughters Mona Maya and Nada Aya,

my parents, and all family members

for supporting me during the hard times, by their prayers and love.
Acknowledgments

I wish to express my sincere and deep gratitude to my supervisor Prof. Dr. -Ing. G. Kompa, for supporting me and giving me the opportunity to carry out this research work at the Department of Microwaves Electronics (MiCEL) (formerly, High Frequency Engineering-HFT), University of Kassel. His moral, intellectual guidance and advices during the course of this work has been inspiring.

I am indebted to Prof. Dr. -Ing. A. Bangert, for his continuous support and help during the thesis achievements, and for accepting to be my second examiner.

Also, I am grateful to Prof. Dr. J. Börcsök and Prof. Dr. B. Witzigmann for their acceptance to evaluate this work and being members in the disputation committee.

Special thank goes to Dr. M. Djebari for his support and help during the achievement of this work. My sincere thanks are directed to my colleagues, Mr. J. A. Zamudio, Mr. A. H. Abbas, Ms. R. Ghahremani, Mr. R. Chatim, Mr. R. Hadi, Dipl. -Ing. B. Wittwer, Mrs. H. Nauditt and Mr. C. Sandhagen, without forgetting recently graduated colleagues, Dr. E. S. Mengistu, Dr. E. R. Srinidhi, Dr. A. Z. Markos, Dr. R. Ma, and Dr. M. S. H. Monsi. Their kind cooperation and support during this thesis is highly appreciated.

Samir Dahmani

Kassel, November 2011
## Contents

List of Figures ........................................................................................................................ vii  
List of Tables .......................................................................................................................... xi  
List of Abbreviations ............................................................................................................. xii  
List of Symbols ..................................................................................................................... xiv  
Abstract ................................................................................................................................... xvi  
Zusammenfassung ............................................................................................................. xviii  

### Chapter 1: Introduction  1  
1.1 RF High Power Amplifiers Requirements for BTS ............................................................. 2  
1.2 AlGaN/GaN HEMTs on SiC Advantages for HPAs ............................................................. 3  
1.3 AlGaN/GaN HEMTs Large-Signal Model Challenges ......................................................... 4  
1.4 Previous Contributions in our Department ...................................................................... 5  
1.5 Proposed Large-Signal Model Enhancement ................................................................... 6  
1.6 Thesis Organization .......................................................................................................... 7  
References .............................................................................................................................. 9  

### Chapter 2: AlGaN/GaN HEMT Fundamentals  14  
2.1 State-of-the-Art AlGaN/GaN HEMTs ..............................................................................15  
2.2 GaN Material Properties.................................................................................................17  
2.3 AlGaN/GaN HEMT Operation Principle ..........................................................................19  
   2.3.1 Piezoelectric Polarization ........................................................................................... 20  
   2.3.2 Spontaneous Polarization ......................................................................................... 22  
2.4 Trapping Mechanisms and Current Collapse ................................................................... 22  
   2.4.1 Surface States (Surface Traps) .................................................................................. 24  
   2.4.2 Buffer States (Deep Traps) ...................................................................................... 25  
2.5 Thermal Properties of HEMTs ........................................................................................ 26  
2.6 AlGaN/GaN HEMT Technology Issues ............................................................................ 27  
   2.6.1 Substrate ................................................................................................................... 27  
   2.6.2 Epitaxy ....................................................................................................................... 28  
   2.6.3 Access Region .......................................................................................................... 29  
References ............................................................................................................................30  

### Chapter 3: AlGaN/GaN HEMT Thermal Modeling and Analysis  35  
3.1 HEMT Thermal Model Formulation Fundamentals ............................................................ 35  
   3.1.1 Thermal Resistance Definition .................................................................................. 36  
   3.1.2 Thermal Capacitance Definition .............................................................................. 37  

References ..............................................................................................................................................
3.1.3 Thermal Model Implementation in CAD .......................................................... 38
3.2 Thermal Analysis of AlGaN/GaN HEMT Structure ........................................... 39
  3.2.1 Thermal Conductivity Degradation in HEMTs ................................................. 40
  3.2.2 AlGaN/GaN HEMT Structure ................................................................. 41
  3.2.3 HEMT Structure Thermal Profile Simulations ............................................. 42
3.3 Steady-State Simulation and Thermal Resistance Estimation ....................... 46
3.4 Transient Thermal Simulation and Time Constant Derivation ..................... 49
References ............................................................................................................. 52

Chapter 4: AlGaN/GaN HEMT Small-Signal Modeling ........................................ 54
  4.1 Extrinsic Parameters Extraction ..................................................................... 55
    4.1.1 Extrinsic Measurement-Correlated Starting Values ................................. 56
    4.1.2 Total Branch Capacitances Determination from Low Frequency Data .... 58
    4.1.3 Capacitance Distribution Determination through Iterative Scan ............ 59
    4.1.4 Inductances Values Extraction in the Iterative Scan ......................... 61
    4.1.5 Extrinsic Resistances Estimation in the Iterative Scan .................... 63
    4.1.6 Minimum Error Determination and Reactive Elements Estimation .... 65
    4.1.7 Extrinsic Resistances Starting Value ............................................... 66
  4.2 Verification of Extrinsic Starting Values ....................................................... 68
  4.3 Extrinsic Model Parameters Optimization ................................................... 69
  4.4 Bias-Dependent Intrinsic Parameters Extraction ......................................... 73
    4.4.1 Gate-Source Branch Elements Extraction ........................................... 73
    4.4.2 Gate-Drain Branch Element Extraction ............................................. 74
    4.4.3 Drain-Source Branch Elements Extraction ....................................... 75
References ............................................................................................................. 78

Chapter 5: AlGaN/GaN HEMT Electrothermal Large-Signal Characterization ...... 80
  5.1 Pulsed I(V) Characterization Fundamentals ................................................. 81
    5.1.1 Pulsed Measurements Principle ........................................................... 81
    5.1.2 Pulsed System Set-Up Requirements .................................................. 83
    5.1.3 Pulsed System External Temperature Controller .................................. 84
  5.2 Drain Current and Pulsed I(V) Characterization Fundamentals for Power Amplifiers .................................................. 85
  5.3 Pulsed I(V) Trapping and Self-Heating Dispersive Effects Characterization .... 87
    5.3.1 Gate Trapping Dispersive Effect Characterization ............................ 88
    5.3.2 Drain Trapping Dispersive Effect Characterization .......................... 89
    5.3.3 Thermal Dispersive Effect Characterization .................................. 91
  5.4 Transients and Time Constants Characterization ........................................ 94
    5.4.1 Drain Transient and Time Constant Characterization ....................... 95
    5.4.2 Gate Transient and Time Constant Characterization ....................... 100
    5.4.3 Thermal Transient and Time Constant Characterization ................... 104
5.5 Thermal Resistance Characterization from Pulsed I(V) ................................................108
   5.5.1 Pulsed I(V) Isothermal Curves Overlapping .............................................................108
   5.5.2 Pulsed I(V) and Static DC Curves Crossing .................................................................110
5.6 Thermal Model From Pulsed I(V) Characterization .....................................................113
References ..........................................................................................................................114

Chapter 6: Electrothermal Large-Signal Modeling and Verification for AlGaN/GaN HEMTs 116
6.1 Large-Signal Equivalent Circuit Model Extraction .......................................................117
   6.1.1 Drain Current Modeling ...............................................................................................119
   6.1.2 Nonlinear Charge Sources Modeling .........................................................................124
   6.1.3 Nonlinear Gate Current Modeling ............................................................................125
6.2 Large-Signal Model Implementation in CAD ..............................................................127
6.3 Large-Signal Model Simulation and Verification .........................................................131
   6.3.1 Model S-Parameter Verification ................................................................................131
   6.3.2 Pulsed I(V) Verification ............................................................................................133
   6.3.3 Large-Signal Single-Tone Verification ......................................................................135
   6.3.4 Two-Tone Intermodulation Distortion Prediction .....................................................137
References ..........................................................................................................................142

Chapter 7: Conclusion and Further Work ...........................................................................145
7.1 Conclusion ....................................................................................................................145
7.2 Further Work ................................................................................................................148
List of Figures

2.1 Cross section of the 43 W/mm AlGaN/GaN HEMT with surface passivation and two field plates connected to the gate............................................................... 15
2.2 Basic structure of AlGaN/GaN HEMT and related conduction band diagram depicting the 2DEG formation................................................................. 20
2.3 Schematic of the crystal structure of the growth orientation, Ga-face and N-face GaN crystal......................................................................................... 21
2.4 Polarization electric field for a strained AlGaN crystal grown on relaxed GaN (Ga-face crystal), (a) large piezoelectric electric field, (b) spontaneous electric field........... 21
2.5 Dependence of the 2DEG sheet density on AlGaN layer thickness, experimental data (marker), least-square linear fit (solid line).................................................. 23
2.6 Dependence of the 2DEG sheet density on Al mole fraction (x) in Al_{x}Ga_{1-x}N compound material, experimental data (marker), least-square linear fit (thin solid line), and with barrier height of 1.42V (dotted line)........................................ 23
2.7 AlGaN/GaN HEMT structure illustrating polarization, trapping mechanisms, and buffer current conduction with their impact on 2DEG electrons......................... 24
2.8 AlGaN/GaN HEMT physical quantities dependency on channel temperature, (a) electron mobility, (b) electron velocity......................................................... 26
2.9 AlGaN/GaN HEMT on SiC structure topology............................................. 27
3.1 Heat conduction and dissipation in semiconductor materials ......................... 36
3.2 Thermal sub-circuit representation in large-signal model of AlGaN/GaN HEMTs to determine channel temperature, (a) First order, (b) Third-order low-pass filter......... 39
3.3 GaN epitaxial layers and SiC substrate thermal conductivity degradation with temperature in AlGaN/GaN HEMTs...................................................... 41
3.4 AlGaN/GaN HEMT structure of the transistor investigated in this work, simulated layers (Sn/Au/SiC/GaN/AlGaN)................................................................ 41
3.5 A two-dimensional cross-sectional area of the thermal profile of an 8-finger structure (8 x 400 µm HEMT)................................................................. 44
3.6 Non-uniform thermal distribution. The temperature gradient is higher at the channel under the gate in the middle fingers as compared to the lateral fingers............. 44
3.7 Thermal mismatch at layers interfaces due to difference in the nonlinear temperature dependency of thermal conductivities (not real scale),.............................. 45
3.8 Thermal mismatch shown at the interface between GaN/SiC for a realistic HEMT structure by evaluating the temperature gradient. Layers have nonlinear temperature dependent thermal conductivities............................................... 45
3.9 Temperature profile at the interface between the AlGaN barrier layer and the GaN buffer layer (AlGaN/GaN) at the 2DEG channel level under the fingers............. 47
3.10 Temperature profile at the interface between the SiC substrate and the GaN buffer layer (GaN/SiC) for the 3.2-mm (8 x 400 µm) HEMT device .................................................. 47
3.11 Equivalent thermal resistance for each individual finger in the 3.2-mm HEMT device with 10 W total dissipated power, on-wafer package considered (Sn, Au).......................... 48
3.12 Total thermal resistance as function of dissipated power density (with Au, Sn) ........ 48
3.13 Transient simulated temperature and exponential fitting: (a) the channel under individual fingers, (b) 2nd order fitting and inset shows fast transient at 1 µsec range... 50
3.14 Transient thermal profile depicting fast and saturation variations for 3.2-mm HEMT (a) at the SiC substrate interface to AlGaN layer, (b) at the surface under the gate fingers (channel temperature). Δt = 50 µs .......................................................... 51
4.1 22-element small-signal distributed equivalent circuit model .................................. 55
4.2 Measurement-Correlated Extrinsic Starting Values Diagram .................................. 57
4.3 22-element distributed model under pinch-off ......................................................... 58
4.4 Cold pinch-off capacitance equivalent circuit model at low frequency .................. 59
4.5 Cold pinch-off T-network equivalent circuit representation of 22-element model..... 60
4.6 Cold pinch-off Z-network equivalent circuit representation after deembedding the pad capacitances C_pgs, C_pds, and C_gda ................................................................. 62
4.7 Cold pinch-off Z-network equivalent circuit representation after deembedding C_pgs, C_pds, and C_gda with correction terms discarded .................. 62
4.8 Cold pinch-off inductance estimation from Z-network equivalent circuit for 0.5 µm AlGaN/GaN HEMT with 3.2-mm (8 x 400 µm) gate width................................. 63
4.9 The equivalent pinch-off stripped Y-parameter network used for deembedding inter-electrode capacitances .......................................................... 64
4.10 Cold pinch-off measurements based series extrinsic resistances estimation for iterative scan through slope evaluation of presented curves ...................... 65
4.11 Evaluation of minimum residual error between cold pinch-off S-parameter measurements and simulations for reactive elements starting values estimation ...... 66
4.12 Cold forward measurements based series extrinsic resistances starting values estimation through slope evaluation of presented curves of a 8 x 400 µm gate width AlGaN/GaN HEMT and 0.5 µm gate-length on SiC................................. 67
4.13 Cold pinch-off S-parameter verification. Comparison between S-parameter measurement and simulation using estimated starting values of small-signal model... 68
4.14 Cold forward S-parameter verification. Markers denote measured, lines denote simulated using estimated starting values of small-signal model.......................... 69
4.15 Pinch-off S-parameter fitting with optimized element values equivalent circuit model. Markers denote measured, lines denote simulated optimized parameters .... 72
4.16 Extracted bias-dependent capacitances (C_ggs, C_gdb, C_db) and transconductance (G_m) as a function of the extrinsic voltages ................................................. 77
4.17 Extracted R_s, R_gdb, G_db, and τ as a function of the extrinsic voltages .................. 77
5.1 Pulsed I(V) fundamentals used for AlGaN/GaN HEMT characterization ............... 82
5.2 Typical FET drain current response in a pulsed measurement system. The current in region III may decrease or increase depending on the dispersion effect present at selected quiescent bias and pulsed-to points ........................................ 83
5.3 Pulsed I(V) measurements to characterize surface trapping. [Solid lines: Quiescent point (0V, 0V); symbols: Quiescent point (0V, -6V)]

5.4 Pulsed I(V) measurements to characterize buffer trapping. Symbols: Quiescent point (-6V, 0V); solid lines: Quiescent point (-6V, 54V)

5.5 Pulsed I(V) measurements to characterize the self-heating at high quiescent dissipated power in comparison with zero quiescent dissipated power. Symbols: Quiescent point (0V, 0V); solid lines: (-2.7V, 40V)

5.6 Pulsed I(V) measurements as function of chuck temperature to characterize the self-heating effect: 20°C (red), 50°C (blue), and 100°C (green) [quiescent bias point is (V_{DS0} = 0V, V_{GS0} = 0V)]

5.7 Buffer trapping time constant: Measured drain current transients from bias points with fixed gate voltage with negligible power dissipation, (a) 1-ms time interval (b) 45-µs time interval [bias (-2V, 0V), pulsed-to (-2V, 1V)]

5.8 Buffer trapping time constant: Measured drain current transients from bias points with fixed gate voltage with higher rating current, (a) 1 ms range (b) 45 µs range [Bias (-0.5V, 0V), pulsed-to (-0.5V, 3V)]

5.9 Buffer trapping time constant from first-order exponential curve fitting parameters: (a) pulsed from bias point (-2V, 0V) to pulsed-to bias point (-2V, 1V) (τ_{DT} = 1.3 µs) and (b) pulsed from (-0.5V, 0V) to pulsed-to bias (-0.5V, 3V) (τ_{DT} = 1 µs)

5.10 Surface trapping time constant: Measured drain current transients from bias points with fixed drain voltage with low power dissipation, (a) 1-ms time interval (b) 200-µs time interval [Bias (-6V, 1V), pulsed-to (-1V, 1V)]

5.11 Surface trapping time constant: Measured drain current transient for bias points with fixed drain voltage with higher power dissipation point [Bias (-6V, 3V), pulsed-to (-2V, 3V)]

5.12 Surface trapping time constant extraction: Measured drain current transient for bias points with fixed drain voltage with low power dissipation. Solid line: First order exponential curve fit with τ_{GT} = 6 µs; Symbols: Measured data [Bias (-6V, 1V), pulsed-to (-1V, 1V)]

5.13 Surface trapping time constant extraction: Measured drain current transient for bias points with fixed drain voltage with higher power dissipation point. τ_{GT} = 14.6 µs; [Bias (-6V, 3V), pulsed-to (-2V, 3V)]

5.14 Thermal time constant characterization: Evolution of measured drain current transients [(V_{GS0}, V_{DS0}) = (-1.5V, 0V) pulsed-to point (v_{GS}, v_{DS}) = (-1.5V, 1V : 7V)]

5.15 Thermal time constant characterization: Transient drain current measurement (stars) and first order exponential function curve fit (solid line), bias (V_{GS0}, V_{DS0}) = (-1V, 0V) and pulsed-to (v_{GS}, v_{DS}) = (-1V, 8V). Inset for 0 < t < 200 µs

5.16 Thermal time constant characterization as function of the equivalent RC circuit order: (a) Linear time scale, (b) logarithmic time scale. Transient drain current measurement (symbols), and 1st, 3rd and 5th order curve fit (solid lines) [Bias point (V_{GS0}, V_{DS0}) = (-1V, 0V) and pulsed-to point (v_{GS}, v_{DS}) = (-1V, 8V)]

5.17 Thermal resistance extraction from overlapped pulsed I(V) curves

5.18 Thermal resistance extraction at the intersection point between Pulsed I(V) cure and static DC curve

5.19 Thermal resistance extraction from pulsed I(V) measurement for fixed-gate current
6.1 Intrinsic large-signal model topology for AlGaN/GaN HEMT including characterized higher-order self-heating sub-circuit (3rd order shown) and characterized buffer and surface trapping sub-circuits ................................................................. 117

6.2 Extracted bias-dependent dispersive drain current model fitting parameters: (a) isothermal drain current, (b) buffer trapping parameter, (c) surface trapping parameter and (d) thermal parameter ........................................................................ 124

6.3 Calculated gate charge sources (a) $Q_{gs}$ and (b) $Q_{gd}$ versus intrinsic voltages .................................................. 125

6.4 Extracted nonlinear gate current sources as function of intrinsic drain and gate voltages, (a) $I_{gs}$ and (b) $I_{gd}$ ................................................................. 126

6.5 Electrothermal large-signal model, (a) complete electrothermal model, (b) intrinsic large-signal model and (c) 3rd order sub-circuit thermal model ....................................................... 128

6.6 Implementation of the large-signal GaN HEMT model in ADS® software: (a) large-signal extrinsic lumped elements and intrinsic symbolically defined device (SDD) implementation including the 5th order thermal sub-circuit, (b) Sample of data access component (DAC) ............................................................................................................. 130

6.7 Large-signal model S-parameter verification at deep class-AB point ($V_{GS0} = -3.4V$, $V_{DS0} = 45V$, $I_{DS0} = 25 mA$) .................................................................................................................. 132

6.8 Large-signal model S-parameter verification at active class-AB point ($V_{GS0} = -2.4V$, $V_{DS0} = 45V$) .............................................................................................................. 132

6.9 Large-signal model S-parameter verification active point ($V_{GS0} = -2.8V$, $V_{DS0} = 25V$). .............................................................................................................. 133

6.10 Pulsed I(V) verification: (Solid lines) model simulation, (dashed lines) measurements, and (dots) model implementation as in [2] for pulsed-to-gate voltage range of ($V_{GS} = -3.3V$ to 0.3V; step 0.6V) ...................................................................... 134

6.11 Single-tone power sweep at class-AB bias point ($V_{GS0} = -2.7V$, $V_{DS0} = 45V$, $I_{DS0} = 300 mA$) at 2.14 GHz with a 50Ω source and load termination: (a) fundamental tone output power, (b) 2nd harmonic output power, (c) 3rd harmonic output power, (d) fundamental output power, gain and power added efficiency ..................... 136

6.12 Two-tone signal response for class-AB operation conditions ($V_{GS0} = -2.7V$, $V_{DS0} = 40V$, $I_{DS0} = 300 mA$) with $f_0$ =2.14 GHz and $\Delta f$ = 200 kHz in a 50Ω source and load environment: (a) Fundamental output power and (b) gain .................................................................. 138

6.13 Two-tone signal response comparison between results obtained by: (a) Procedure presented in this work and (b) previous procedure as described in [2]. Measurement (symbols) and simulation (lines) for ($V_{GS0} = -2.7V$, $V_{DS0} = 40V$, $I_{DS0} = 300 mA$) with $f_0$ =2.14 GHz and $\Delta f$ = 200 kHz in a 50Ω environment ................................................. 139

6.14 Two-tone signal response for class-AB operation conditions ($V_{GS0} = -3V$, $V_{DS0} = 45V$, $I_{DS0} = 190 mA$) with $f_0$ =2.14 GHz and $\Delta f$ = 200 kHz in a 50Ω source and load environment. (a) Fundamental output power, (b) gain, and (c) IMD3 output power ............................................ 140

6.15 Two-tone signal response for deep class-AB operation conditions ($V_{GS0} = -3.47V5$, $V_{DS0} = 40V$, $I_{DS0} = 25 mA$) with $f_0$ =2.14 GHz and $\Delta f$ = 200 kHz in a 50Ω source and load environment: (a) Variation in channel temperature estimation ($\Delta T_{ch}$), (b) fundamental output power, (c) gain, and (d) IMD3 output power ................................................. 141

6.16 Two-tone signal response comparison between results obtained by: (a) Enhanced procedure presented in this work and (b) previous procedure in [2] for ($V_{GS0} = -3.47V5$, $V_{DS0} = 40V$, $I_{DS0} = 25 mA$ ≈ 10% of $I_{DS}$) with $f_0$ =2.14 GHz and $\Delta f$ = 200 kHz in a 50 Ω environment ................................................. 142
List of Tables

2.1 State of the Art GaN HEMTs for RF power applications.............................. 16
2.2 Sample of commercial power GaN HEMTs for RF amplifiers......................... 16
2.3 Semiconductors material properties figure of merit [17] [18]............................... 18
2.4 Wide bandgap material advantages for power amplifier applications............... 19
4.1 Starting parameter values of a 3.2-mm AlGaN/GaN HEMT with an 8 x 400 μm gate-width derived from measurement (pinch-off and forward).......................... 67
4.2 Optimized parameter values of a 3.2-mm (8 x 400 μm) GaN HEMT.................. 71
5.1 Thermal time constants for 3.2-mm AlGaN/GaN HEMTs on SiC.......................... 108
5.2 Thermal resistances for 3.2-mm AlGaN/GaN HEMTs on SiC............................. 114
5.3 Thermal capacitances for 3.2-mm AlGaN/GaN HEMTs on SiC............................ 114
# List of Abbreviations and Acronyms

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2DEG</td>
<td>Two-Dimensional Electron Gas</td>
</tr>
<tr>
<td>3G, 4G</td>
<td>Third (Fourth) Generation</td>
</tr>
<tr>
<td>ACPR</td>
<td>Adjacent Channel Power Ratio</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System software</td>
</tr>
<tr>
<td>AlGaN</td>
<td>Aluminum Gallium Nitride</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
</tr>
<tr>
<td>BTS</td>
<td>Base Transceiver Station</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CW</td>
<td>Continuous Wave</td>
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<tr>
<td>DAC</td>
<td>Data Access Component in ADS software</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
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<tr>
<td>DiVA</td>
<td>Dynamic I(V) Analyzer</td>
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<tr>
<td>DPD</td>
<td>Digital Predistortion</td>
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<tr>
<td>EER</td>
<td>Envelope Elimination and Restoration</td>
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<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>G-FP</td>
<td>Gate Field Plate</td>
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<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
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<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
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<tr>
<td>HPA</td>
<td>High Power Amplifier</td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation Distortion</td>
</tr>
<tr>
<td>IMD3</td>
<td>Third Order Intermodulation Distortion</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Laterally Diffused Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>LTE-A</td>
<td>Long Term Evolution – Advanced</td>
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<tr>
<td>LUT</td>
<td>Look-up Table in ADS</td>
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<tr>
<td>MAG</td>
<td>Maximum Available Gain</td>
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<tr>
<td>MESFET</td>
<td>MEtal-Semiconductor FET</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal-Organic Chemical Vapor Deposition</td>
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<tr>
<td>MSG</td>
<td>Maximum Stable Gain</td>
</tr>
<tr>
<td>MTA</td>
<td>Microwave Transition Analyzer</td>
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<td>MWO</td>
<td>Microwave Office</td>
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<tr>
<td>OPEX</td>
<td>Operational Expense</td>
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<tr>
<td>OFDM</td>
<td>Orthogonal Frequency Division Multiplex</td>
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<tr>
<td>PA</td>
<td>Power Amplifier</td>
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<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
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<td>PAR</td>
<td>Peak-to-Average Ratio</td>
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<td>PEP</td>
<td>Peak Envelope Power</td>
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<tr>
<td>PM</td>
<td>Phase Modulation</td>
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<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
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<tr>
<td>PSK</td>
<td>Phase Shift Keying</td>
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<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>SDD</td>
<td>Symbolically Defined Device</td>
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<tr>
<td>S-FP</td>
<td>Source Field Plate</td>
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<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>TEC</td>
<td>Thermal Expansion Coefficient</td>
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<tr>
<td>UMTS</td>
<td>Universal Mobile Telecommunications System</td>
</tr>
<tr>
<td>VNA, VSA</td>
<td>Vector Network Analyzer, Vector Signal Analyzer</td>
</tr>
<tr>
<td>W-CDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
<tr>
<td>WiMAX</td>
<td>Worldwide Interoperability for Microwave Access</td>
</tr>
<tr>
<td>WirelessMAN</td>
<td>Wireless Metropolitan Area Network</td>
</tr>
</tbody>
</table>
### List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gs}$, $C_{ds}$, $C_{gd}$</td>
<td>Intrinsic gate-source, drain-source, gate-drain capacitances</td>
<td>F</td>
</tr>
<tr>
<td>$C_{gs0}$, $C_{ds0}$, $C_{gd0}$</td>
<td>Gate-source, drain-source and gate-drain total capacitances of a ‘cold-FET’ biased below pinch-off</td>
<td>F</td>
</tr>
<tr>
<td>$C_{pdi}$, $C_{pgi}$, $C_{gdi}$</td>
<td>Inter-electrode capacitances</td>
<td>F</td>
</tr>
<tr>
<td>$C_{pga}$, $C_{pda}$, $C_{gda}$</td>
<td>Parasitic pad capacitances</td>
<td>F</td>
</tr>
<tr>
<td>$C_{th}$</td>
<td>Thermal capacitance</td>
<td>s·W/K</td>
</tr>
<tr>
<td>$C_{GT}$, $C_{DT}$</td>
<td>Trapping capacitances in RC model for trapping constants</td>
<td>F</td>
</tr>
<tr>
<td>$c_{0}$</td>
<td>Velocity of light</td>
<td>cm/sec</td>
</tr>
<tr>
<td>$E$</td>
<td>Electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>$E_F$</td>
<td>Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>$E_C$</td>
<td>Bottom edge of conduction band</td>
<td>eV</td>
</tr>
<tr>
<td>$f_t$</td>
<td>Current gain cutoff frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>Power gain cutoff frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_D$</td>
<td>Function modeling traps associated with deep-level</td>
<td>A/V</td>
</tr>
<tr>
<td>$f_G$</td>
<td>Function modeling traps associated with surface state</td>
<td>A/V</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Function modeling self-heating effects</td>
<td>A/K</td>
</tr>
<tr>
<td>$G$</td>
<td>Power gain</td>
<td>dB</td>
</tr>
<tr>
<td>$G_{ds}$</td>
<td>Drain-to-source conductance</td>
<td>S</td>
</tr>
<tr>
<td>$G_{fs}$, $G_{gs}$</td>
<td>Differential gate-source diode conductance</td>
<td>S</td>
</tr>
<tr>
<td>$G_{gd}$, $G_{gd}$</td>
<td>Differential gate-drain diode conductance</td>
<td>S</td>
</tr>
<tr>
<td>$G_m$</td>
<td>Channel transconductance</td>
<td>S</td>
</tr>
<tr>
<td>$I_{DC}$, $I_{DS,iso}$</td>
<td>Isothermal drain-source DC current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Saturated drain-source current (zero gate bias voltage)</td>
<td>A</td>
</tr>
<tr>
<td>$I_{gs}$, $I_{ds}$</td>
<td>Intrinsic gate-source and drain-source current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{GS}$, $I_{DS}$</td>
<td>Extrinsic gate-source and drain-source current</td>
<td>A</td>
</tr>
<tr>
<td>$i_{GS}$, $i_{DS}$</td>
<td>Pulsed DC gate-source and drain-source current</td>
<td>A</td>
</tr>
<tr>
<td>$I_{max}$</td>
<td>Maximum drain-source current (gate-forward bias)</td>
<td>A</td>
</tr>
<tr>
<td>$L_{g}$, $L_{d}$, $L_{s}$</td>
<td>Gate, drain, and source inductance</td>
<td>H</td>
</tr>
<tr>
<td>$L_G$</td>
<td>Gate length</td>
<td>µm</td>
</tr>
<tr>
<td>$L_{DS}$, $L_{GS}$, $L_{GD}$</td>
<td>Drain-source, gate-source and gate-drain spacing</td>
<td>µm</td>
</tr>
<tr>
<td>$B V_{gd}$</td>
<td>Gate-drain breakdown voltage</td>
<td>V</td>
</tr>
<tr>
<td>$n_s$</td>
<td>Sheet charge concentration ($\sigma q$)</td>
<td>cm$^{-2}$</td>
</tr>
<tr>
<td>$p$</td>
<td>Power back-off</td>
<td>W</td>
</tr>
<tr>
<td>$PAE_{total}$</td>
<td>Power added efficiency, total power added efficiency</td>
<td>%</td>
</tr>
<tr>
<td>$P_{DC}$, $P_{dc,av}$, $P_{dc}(t)$</td>
<td>DC, average, instantaneous dissipated power</td>
<td>W</td>
</tr>
<tr>
<td>$P_{in}$, $P_{in,av}$</td>
<td>RF input power, average input power</td>
<td>W</td>
</tr>
<tr>
<td>$P_{out}$, $P_{out,av}$</td>
<td>Output power, average output power</td>
<td>W</td>
</tr>
<tr>
<td>$P_{PE}$</td>
<td>Piezoelectric polarization induced charge density</td>
<td>C/cm$^2$</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>$P_{SP}$</td>
<td>Spontaneous polarization induced charge density</td>
<td>C/cm²</td>
</tr>
<tr>
<td>$q$</td>
<td>Electron charge (1.602x10⁻¹⁹C)</td>
<td></td>
</tr>
<tr>
<td>$Q_{gs}, Q_{gd}$</td>
<td>Gate-source and gate-drain charges</td>
<td></td>
</tr>
<tr>
<td>$R_{th}$</td>
<td>Thermal resistance</td>
<td>K/W</td>
</tr>
<tr>
<td>$R_g, R_s, R_o, R_c$</td>
<td>Gate, drain, source, and channel resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{gs}, R_{gd}$</td>
<td>Gate-source and gate-drain charging resistances</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{GT}, R_{DT}$</td>
<td>Part of an RC network to model trapping time constants</td>
<td>Ω</td>
</tr>
<tr>
<td>$S_{ij}$</td>
<td>Two-port scattering parameters (i, j = 1,2)</td>
<td></td>
</tr>
<tr>
<td>$V_{br}$</td>
<td>Breakdown voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS0}, V_{DS0}$</td>
<td>Bias gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}, V_{DS}$</td>
<td>Extrinsic gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{gs}, V_{ds}$</td>
<td>Intrinsic gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_k$</td>
<td>Knee voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_P$</td>
<td>Pinch-off gate-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_s$</td>
<td>Saturation velocity</td>
<td>cm/s</td>
</tr>
<tr>
<td>$Y_{ij}$</td>
<td>Two-port small-signal admittance parameters (i, j = 1,2)</td>
<td>S</td>
</tr>
<tr>
<td>$Z_L$</td>
<td>Load impedance</td>
<td>Ω</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>Characteristic impedance</td>
<td>Ω</td>
</tr>
<tr>
<td>$Z_{out}, Z_{in}$</td>
<td>Output and input impedances</td>
<td>Ω</td>
</tr>
<tr>
<td>$s$</td>
<td>Gate-pitch (gate-to-gate spacing)</td>
<td>μm</td>
</tr>
<tr>
<td>$S_{ij}$</td>
<td>Scattering parameters</td>
<td></td>
</tr>
<tr>
<td>$T_0$</td>
<td>Ambient temperature</td>
<td>K</td>
</tr>
<tr>
<td>$T_{chuck}$</td>
<td>Chuck (back-plate) temperature</td>
<td>K</td>
</tr>
<tr>
<td>$T_{ch}$</td>
<td>Channel temperature</td>
<td>K</td>
</tr>
<tr>
<td>$v_s$</td>
<td>Saturation velocity</td>
<td>cm/s</td>
</tr>
<tr>
<td>$v_{GS}, v_{DS}$</td>
<td>Pulsed DC gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS0}, V_{DS0}$</td>
<td>Bias gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}, V_{DS}$</td>
<td>Terminal gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_{gs}, V_{ds}$</td>
<td>Intrinsic gate-source and drain-source voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_P$</td>
<td>Gate-source pinch-off voltage</td>
<td>V</td>
</tr>
<tr>
<td>$W_G$</td>
<td>Gate width</td>
<td>μm</td>
</tr>
<tr>
<td>$Y_{ij}$</td>
<td>Small-signal admittance parameters</td>
<td>S</td>
</tr>
<tr>
<td>$Z_{gs}, Z_d, Z_s$</td>
<td>Intrinsic gate, drain, and source branch impedance</td>
<td>Ω</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>Small-signal impedance parameters</td>
<td>Ω</td>
</tr>
<tr>
<td>$\Delta T_{ch}$</td>
<td>Change in channel temperature</td>
<td>K</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>Relative dielectric permittivity</td>
<td></td>
</tr>
<tr>
<td>$\eta_d, \eta_{avg}$</td>
<td>Drain Efficiency, average drain efficiency</td>
<td>%</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>Thermal conductivity</td>
<td>W/cm·K</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Electron mobility</td>
<td>cm²/V·s</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Sheet charge density</td>
<td>C/cm²</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Transit delay time</td>
<td>s</td>
</tr>
<tr>
<td>$\phi_b$</td>
<td>Barrier height</td>
<td>V</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Transit delay time</td>
<td>s</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular frequency</td>
<td>rad·Hz</td>
</tr>
</tbody>
</table>
Abstract

The rapid growth in high data rate communication systems has introduced new high spectral efficient modulation techniques and standards such as LTE-A (long term evolution-advanced) for 4G (4th generation) systems. These techniques have provided a broader bandwidth but introduced high peak-to-average power ratio (PAR) problem at the high power amplifier (HPA) level of the communication system base transceiver station (BTS). To avoid spectral spreading due to high PAR, stringent requirement on linearity is needed which brings the HPA to operate at large back-off power at the expense of power efficiency. Consequently, high power devices are fundamental in HPAs for high linearity and efficiency. Recent development in wide bandgap power devices, in particular AlGaN/GaN HEMT, has offered higher power level with superior linearity-efficiency trade-off in microwaves communication.

For cost-effective HPA design to production cycle, rigorous computer aided design (CAD) AlGaN/GaN HEMT models are essential to reflect real response with increasing power level and channel temperature. Therefore, large-size AlGaN/GaN HEMT large-signal electrothermal modeling procedure is proposed. The HEMT structure analysis, characterization, data processing, model extraction and model implementation phases have been covered in this thesis including trapping and self-heating dispersion accounting for nonlinear drain current collapse.

The small-signal model is extracted using the 22-element modeling procedure developed in our department. The intrinsic large-signal model is deeply investigated in conjunction with linearity prediction. The accuracy of the nonlinear drain current has been enhanced through several issues such as trapping and self-heating characterization. Also, the HEMT structure thermal profile has been investigated and corresponding thermal resistance has been extracted through thermal simulation and chuck-controlled temperature pulsed I(V) and static DC measurements. Higher-order equivalent thermal model is extracted and implemented in the HEMT
large-signal model to accurately estimate instantaneous channel temperature. Moreover, trapping and self-heating transients has been characterized through transient measurements. The obtained time constants are represented by equivalent sub-circuits and integrated in the nonlinear drain current implementation to account for complex communication signals dynamic prediction.

The obtained verification of this table-based large-size large-signal electrothermal model implementation has illustrated high accuracy in terms of output power, gain, efficiency and nonlinearity prediction with respect to standard large-signal test signals.
Zusammenfassung


Die Verifikation des entwickelten tabellenbasierten elektrothermischen Großsignalmodells für großflächige Leistungstransistoren zeigt eine hohe Genauigkeit hinsichtlich Ausgangsleistung, Verstärkung, Wirkungsgrad sowie bei der Simulation von üblichen Großsignaltestsignalen.
Chapter 1

Introduction

In the last few years, the modern microwave wireless digital communications has reached unrecorded acceleration in systems innovation, circuit design techniques and related technology development. Actual and future designs and technology should meet the tremendous users market demand and reduce the increasing operation cost for actual systems such as Worldwide interoperability for Microwave Access (WiMAX), Wireless Local Area Networks (WLAN), cellular infrastructure, satellite communications and military communications. The main characteristics of these systems are the use of high data rate transmission techniques and novel development strategies in both device level and architectures for more cost effectiveness. For increasing user capacity satisfaction, efficient broadband spectral modulation techniques are employed. Techniques such as, Phase Shift Keying (PSK) and Quadrature Amplitude Modulations (QAM) are used in Wide-band Code Division Multiple Access (W-CDMA) and Orthogonal Frequency Division Multiple Access (OFDMA) modulations [1].

Therefore, modern communication systems should have base transceiver station (BTS) with high power amplifiers (HPAs) satisfying multi-carrier complex modulation schemes. These spectrum efficient modulations result in a non-constant envelope signal. This increase in bandwidth efficiency necessitates an increase in dynamic range (large back-off operation), which is essential for communication systems designers. High peak power to average ratio (PAR) is of great interest for future LTE (LTE-A) and 4G standards. It deteriorates HPA average power efficiency; it brings the power amplifier to work at low efficiency region to avoid spectral spreading [2].
1.1 RF High Power Amplifiers Requirements for BTS

High power RF amplifiers (HPAs) are considered as the central element in today’s wireless electronic communications. Due to the continuous increase in wireless communications, Base Transceiver Stations market demand is evaluated to be thousands of units per year [3]. To reduce the cost of the introduced power loss, it is incessantly required to develop HPAs with high linearity, high average efficiency, broad bandwidth, high output power levels, high gain and smaller size with reduced cost. These correlated parameters are very challenging for HPAs designers [4].

For enhanced average power efficiency (higher output power levels operation), HPAs should be inherently investigated and designed for high linearity. This requirement is necessary for determining signal interferences between adjacent modern communication channels [3]. Consequently, HPAs are confined to linearity requirement with conjunction to high average efficiency through three possible strategies [5],

- At system level, HPA linearity is optimized through the introduction of linearization techniques, such as feedback, feedforward and predistortion on the available HPA. As a requirement for these techniques, the HPA should have bandwidth independent nonlinearity (i.e. minimum memory effect) [6]. The bandwidth of the HPA should increase with improved circuit design methods including the matching and bias circuits in the amplifier [7].

- At circuit level, linearity can be improved by improving actual designs or developing novel complex design architectures. Circuit level linearization can be implemented using techniques like derivative superposition [8], while techniques such as Doherty, outphasing, envelope elimination and restoration (EER), envelope tracking (ET) and Class-S amplifier with $\Delta-$Σ modulator are used to enhance efficiency at large power back-off [7]. Both preceded linearization techniques suffer from added cost, increased size, reduced effective bandwidth.

- Finally, at the device level, the key component of the HPA linearity is the power device used. Its related processes and technology have a great effect on linearity. The use of GaN technology with field plate structure has increased significantly HPAs linearity [9] [10]. Also, the availability of GaN low on-resistance and high power devices
enhances the average efficiency by avoiding power-combining schemes for multiple-devices HPAs. Furthermore, reduced technology dependent leakage current has lead to increased HPA power efficiency [11]-[13].

1.2 AlGaN/GaN HEMTs on SiC Advantages for HPAs

From technology consideration, the design trend for future high performance HPAs are oriented towards the use of very high output power level and stable active devices. For current basestation HPAs, the used device technology is still Si-LDMOS in BTS manufacturing. Available power devices, Si-LDMOS FET and GaAs MESFET, could not be candidate for future systems requirements due to their reached technology limits in broadband operation, power handling capability, thermal stability, gain, and power efficiency [14]. Recently, new promising wide bandgap material device technologies, SiC MESFET and AlGaN/GaN high electron mobility transistors (HEMTs) on Si and SiC substrates, start to get into the power devices market [15].

AlGaN/GaN HEMT devices on SiC substrate have shown the highest figure of merit regarding HPAs performances (linearity, gain, efficiency, large input and output impedances) [3]. It has improved HPAs by a factor of more than 10 in power densities as compared to other material technologies based on GaAs or silicon. Its high sheet carrier density and the high saturation electron velocity enabled the highest output power level [16]. Average power efficiency is enhanced due to low-on resistance significantly related to GaN HEMT high electron mobility [17]. Very high off-breakdown voltage (1900V) [18] and (10400V) [19], very high output power density (41.4 W/mm) on SiC substrate [15], total output power exceeding 800W [20], high thermal conductivity, excellent thermal stability, and high channel operating temperatures contribute in linearity enhancement at the device level [21]. These AlGaN/GaN HEMTs on SiC-substrate characteristics provide very interesting design benefits to produce highly linear, high efficiency HPA [17]. As an example, GaN-based HPA has reached over 800W output power, 14.0 dB high linear gain and high efficiency of 50% over the wide frequency range of 2.9 - 3.3 GHz, operating at 65 V drain bias voltage under pulsed conditions, at a duty of 10% and pulse width of 200 μs [20]. Another HPA designed around two 48-mm HEMTs has produced a 370W saturation output power and 11.2 dB
linear gain at 2.14 GHz under W-CDMA input signal with 45V drain bias [22].

1.3 AlGaN/GaN HEMTs Large-Signal Model Challenges

Accurate electrothermal nonlinear large-signal model, for GaN-based highly linear high power amplifiers (HPAs) analysis and design in CAD environment, is essential for reduced design-to-production cycle. For modern spectral efficient modern 3G/4G wireless communications HPAs, current dispersion (trapping, self-heating and transient effects), intermodulation distortions and higher-order harmonics should be correctly accounted for to proper nonlinearity analysis and prediction (electrical and thermal memory effect). These key factors require reliable measurement data-base, proper equivalent model representation, and robust complex modeling extraction procedure.

To date, researchers are still looking for advanced modeling procedures for enhancing large-signal electrothermal models for high power AlGaN/GaN HEMT devices with large-periphery gate width in conjunction with HPAs class of operation. Many correlated effects are difficult to characterize and more tedious to capture in the equivalent large-signal model implementation in CAD. Some models describe well the current collapse and fundamental output power, but are deficient in intermodulation distortions and higher harmonics prediction. Most reported large-signal models do not cover linearity prediction capabilities, whereas other models deliver good linearity prediction with poor fundamental output power estimation [23]-[25]. Lookup table-based large-signal model extraction procedure recently developed in our department has proven more accuracy in all aspects due to the robustness of the extraction technique and the more elaborate physically relevant equivalent large-signal model parameters [13]. Issues such as, model consistency, dispersion effects, nonlinear equivalent model data construction (e.g. interpolation and extrapolation problems), nonlinear implementation in CAD simulator, and continuous differentiable nonlinear model parameters was covered. Enhanced large-signal electrothermal modeling strategy will be presented all along this thesis to meet recent large-power large-gate width periphery (3.2-mm) AlGaN/GaN HEMT devices.
1.4 Previous Contributions in our Department

The handled research work in this thesis is a contribution in the long experience that our department has in active device modeling. In [26] and [27] a model parameter extraction technique was proposed based on error-corrected small-signal S-parameter measurements of MESFETs and HEMTs by introducing a new calibration technique for microstrip test-fixtures up to 40 GHz denoted THLR. In [28]-[30] a large-signal characterization technique was developed which enables direct extraction of large-signal model parameters from signal waveforms using a numerical harmonic-balance technique based on active load-pull technique and THLR calibration procedure [31]-[33]. Then, model parameter extraction technique was continuously enhanced as in [34]-[36]. A top-down modeling approach was proposed in [37]; consistent linearized small-signal model was derived from corresponding large-signal model. To overcome small-signal model topology and device structure mismatch, a bottom-up approach was developed starting from physical distributed small-signal equivalent circuit model comprising 20 elements to derive a large-signal model for GaAs active devices [38]. An optimization technique was introduced with automatic generation of starting values from cold pinch-off measurements to determine the small-signal model parameters instead of preceding user intervention techniques. To enhance the optimization technique for AlGaN/GaN HEMT devices, in [13] the small-signal intrinsic part was extended to 22-element equivalent circuit including the gate-forward and gate-breakdown effects to account for high power modeling. Physical-relevant gate-drain equivalent capacitances were introduced due to higher contact resistances in AlGaN/GaN HEMTs, and forward measurement was added to get reliable starting values due to error in pinch-off measurement [39]. Furthermore, to capture model nonlinearity prediction, spline approximation technique was introduced in intrinsic data construction to obtain continuous data and corresponding higher-order derivatives [40]-[42].

Initially the extraction method has been developed and tested for GaAs FETs for low and medium power. Then, it was extended to low and medium power GaN HEMTs. Within the framework of the BMBF (Bundesministerium für Bildung und Forschung) Gallium Nitride program termed “GaN Mobile”, the large-signal extraction and modeling technique so far developed in the department should be revised to be extended to large-size large-power GaN HEMTs. Therefore, with large gate periphery
devices (3.2-mm gate-width), an early compression shows up in RF fundamental output power simulations, also deviation is noticed between simulation and measurement for higher-order harmonics and intermodulation distortion (IMD), mainly at quiescent bias points close to pinch-off or ohmic region. This discrepancy can be associated to three main factors. First is the persisting uncertainty in the measurement mainly at pinch-off [43]-[45] [13], and the limited measurement database which affects compression point value in large-signal RF operating conditions for large current rating devices. Second is the HEMT terminals voltage transformation, processing and mapping in the electrothermal large-signal model extraction procedure. It affects largely the ohmic region; this can be reduced through enhanced data processing routines. The third factor that affects highly large-signal drain current, higher-order harmonics and intermodulation distortion is the thermal and electrical memory effects prediction capability. This has to be improved by including more physical-relevant model elements and sub-circuits to account for large trapping effects and self-heating available in high power large-size AlGaN/GaN HEMT devices; this last factor is very important for power amplifiers nonlinearity prediction and analysis.

1.5 Proposed Large-Signal Model Enhancement

Therefore, the scope of this research work is to extend the large-signal modeling procedure to accurately simulate large-size high power AlGaN/GaN HEMT devices with high self-heating and trapping effects. The model validity region is extended towards the ohmic region and the pinch-off region (deep Class-AB operation conditions) by enhancing the large-signal electrothermal equivalent circuit model extraction and implementation. A rigorous analysis and characterization of the thermal behavior of large gate periphery devices is addressed, from which enhanced higher-order equivalent thermal model implementation is constructed. A better prediction of the static and dynamic channel temperature variation is predicted even at pinch-off region. It increases the nonlinear drain current sensitivity to real instantaneous temperature operating conditions. This improves the model capability to predict accurately thermal memory effect on harmonics and intermodulation distortion terms in modern digital communications modulation standards. Similarly, a deep investigation in surface trapping, buffer trapping, and their transient dispersion effects is
handled. A careful analysis and measurement characterization of the significant trapping dispersion effects and transients has led to the development of a more comprehensive and precise surface and buffer transient trapping equivalent RC model representations. This improves the model capability to predict accurately the electrical memory effect on harmonics and intermodulation distortion terms. The high power large-size AlGaN/GaN HEMT large-signal nonlinear drain current implementation is altered so that it responds correctly to above mentioned effects. Also, enhanced data processing routines are introduced to reduce processing error.

1.6 Thesis Organization

Therefore, the main focus of the work presented in this thesis is to enhance the modeling procedure to be applied accurately for large-signal large-size AlGaN/GaN HEMT devices on SiC substrate (8 x 400 µm gate-width and 0.5 µm gate length) with considerable self-heating and trapping effects. Therefore, accurate intermodulation distortion prediction, implemented large-signal model enhanced convergence, and error reduction between simulated and measured RF electrical parameters and quantities will be shown for highly-linear and high efficiency power amplifiers applications in wireless communications.

To cover the various aspects of the enhanced large-size AlGaN/GaN HEMT large-signal modeling procedure, the thesis is partitioned into seven chapters. In Chapter 1, the motivation and the scope of the research work has been described. A brief description of our department achievements and contribution in transistor modeling is presented. After which the necessity for enhanced and accurate large-signal modeling procedure for high power large-gate periphery AlGaN/GaN HEMT devices (3.2-mm), for highly linear high efficiency power amplifiers applications in modern digital mobile communications, has been addressed.

In Chapter 2, state of the art, material properties, technology key parameters, and modeling approaches are summarized for the high power AlGaN/GaN HEMT devices for power amplifiers applications. The fundamentals of power AlGaN/GaN HEMT technology and characteristics will be introduced. A brief explanation of its main advantages and limiting factors is undertaken in conjunction with modern digital communications power amplifier.
Thermal modeling and simulations of the high power AlGaN/GaN HEMT structure will be addressed in Chapter 3. Fundamentals of heat transfer analysis and related thermal model parameters definitions are first summarized. The thermal model equivalent CAD implementation is extracted through two types of analysis. The equivalent thermal resistance(s) is obtained from the steady state thermal simulation of the AlGaN/GaN HEMT structure, and the equivalent thermal capacitance is deduced from the transient time constant obtained from the transient thermal simulations of the HEMT structure.

In Chapter 4, the small-signal model extraction procedure will be summarized. It is based on the 22-element model developed in our department [13]. The model equivalent extrinsic reactive elements starting values will be extracted through the cold pinch-off S-parameters measurements, then the model equivalent series resistances will be obtained from cold forward S-parameters measurements. These starting values are used in an optimization process to obtain the optimal extrinsic bias-independent parameters, after which the small signal bias-dependent model intrinsic parameters are evaluated. The simulated S-parameters from the constructed small-signal model parameters will be compared to measurements for verification.

To enhance the accuracy and convergence of the large-signal model, the large-size 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT device will be thoroughly characterized under a set of well investigated bias conditions under different ambient temperatures in Chapter 5. In this regard, careful pulsed I(V) measurements based large-signal characterization will be used to identify the device behavior and response under realistic large-signal power amplifiers applications. First, the drain current dispersion effects due to surface trapping, buffer trapping, and self-heating will be quantified through static and dynamic gate and drain voltages with controlled temperatures. Then, the surface and buffer trapping time constants will be determined from transient measurements. These time constants will be used through an enhanced realistic equivalent RC sub-circuit representation in the large-signal model implementation. Similarly, the self-heating time constants will be extracted from transient drain current measurements at appropriate bias conditions. Moreover, the equivalent thermal model resistances will be deduced from appropriate measurements. An enhanced thermal model equivalent higher-order RC sub-circuit is constructed in the large-signal electrothermal model to estimate accurately the channel
temperature in HEMT devices. These measurements based surface, buffer, and self-heating transient sub-circuits will enhance the electrical and the thermal memory effects prediction, and therefore it will increase accuracy in RF power fundamentals, harmonics, and intermodulation distortion terms.

The large-signal electrothermal model parameters and the table-based implementation of the large-size AlGaN/GaN HEMT device in CAD tools will be described in Chapter 6. The large-signal nonlinear gate charges, gate current sources, and drain current will be evaluated from the small-signal parameters of Chapter 4 to maintain model consistency. Data in Chapter 5 for trapping and self-heating dispersion effects characterization will be implemented in the nonlinear ambient temperature dependent drain current look-up tables. Similarly from Chapter 5, measurements based transients data will be implemented directly in corresponding sub-circuits in the large-circuit electrothermal model. Details about the implementation of the large-signal electrothermal model in CAD tools (Advanced Design System) will be included. Verification and validation standard tests for power amplifier applications will be provided to show the consistency, the accuracy, and the convergence of the implemented large-signal electrothermal HEMT model as compared to their corresponding measurements. Finally, summary of the research results and further works will be provided in Chapter 7.

References


Chapter 2

AlGaN/GaN HEMT Fundamentals

In today’s communication systems basestations, high linearity and high efficiency requirements are crucial in high power amplifiers (HPAs). As described in Chapter 1, one of the key strategies to enhance both linearity and efficiency in HPAs, in conjunction with modern spectral modulation techniques requirements (i.e. Long Term Evolution (LTE) and LTE-Advanced), is the choice of power device and technology. AlGaN/GaN HEMTs have shown superior performances over today’s existing commercial power device technologies (i.e. Si-LDMOS and GaAs MESFET). For example, the output power density of GaN HEMT is 10 times more than Si-LDMOS devices [1]. Parameters such as high output power level, thermal stability, linearity, power efficiency, gain and design facility specifications are highly matched by HPAs based on newly commercialized GaN power devices [2].

In the following sections, a brief insight into the new developments in AlGaN/GaN HEMTs material and devices will be presented. The state of art of GaN HEMT will be summarized followed by the main material parameters, HEMT device fundamentals and key advantages for communication systems. Important mechanisms for HPAs and GaN HEMT characterization and modeling such as trapping states and self-heating also have been introduced. Finally, a brief description of device technology process enhancement as correlated to RF power applications performances is covered.
2.1 State-of-the-Art AlGaN/GaN HEMTs

Since the first appearance of the AlGaN/GaN high electron mobility transistor (HEMT) in 1993 [3], the device characteristics and performances have shown great improvements in both frequency and power. In the beginning of 2004, many company introduced HEMT devices on Si-substrate with power handling ranging from 1.9 W/mm at 10 GHz from Tiger Company [4] to 12 W/mm at 2.14 GHz for wireless applications from Nitronex [5].

Similarly for Cree Company, in the early 1999, it has launched a 6.9 W/mm output power density for GaN HEMT on SiC substrate with operating frequency up to 10 GHz [6]. Five years later, it has reached a continuous output power of 32.2 W/mm by the year 2004 with 4 GHz operating frequency at 120V biasing for a device with 0.55 µm x 246 µm with enhanced field plate configuration of 1.1 µm length and reduced trapping effect on SiC substrate. This device was revolutionary with respect to conventional GaN devices with 10-12 W/mm attained values. By changing the field plate length to 0.9 µm, the device achieved 30.6 W/mm at 8 GHz operating frequency [7]. By 2006, a similar device configuration has achieved an output power density of 41.4 W/mm for GaN on SiC substrates with 4 GHz operating frequency at 135V biasing with 16 dB associated gain and 60% PAE [8]. As, presented in Figure 2.1, the structure is formed by a double field plate configuration; the second field plate is constructed on the first field plate with a separation of a second SiN-layer.

Figure 2.1 Cross section of the 43 W/mm AlGaN/GaN HEMT with surface passivation and two field plates connected to the gate. Adopted from [8].
Table 2.1 State of the Art GaN HEMTs for RF power applications.

<table>
<thead>
<tr>
<th>Year – Publication</th>
<th>Manufacturer</th>
<th>Power (W/mm)</th>
<th>Drain Voltage (V)</th>
<th>PAE (%)</th>
<th>Frequency (GHz)</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2005 - HRL-ONR [9]</td>
<td></td>
<td>5.7</td>
<td>20</td>
<td>45</td>
<td>30</td>
<td>SiC</td>
</tr>
<tr>
<td>2005 - ONR [10]</td>
<td></td>
<td>10.5</td>
<td>30</td>
<td>34</td>
<td>40</td>
<td>SiC</td>
</tr>
<tr>
<td>2004 - Cree [7]</td>
<td></td>
<td>32.2</td>
<td>120</td>
<td>54.8</td>
<td>4</td>
<td>SiC</td>
</tr>
<tr>
<td>2006 - Emcore [12]</td>
<td></td>
<td>9.1</td>
<td>55</td>
<td>23.7</td>
<td>18</td>
<td>SiC</td>
</tr>
<tr>
<td>2006 - Cree [8]</td>
<td></td>
<td>41.4</td>
<td>135</td>
<td>60</td>
<td>4</td>
<td>SiC</td>
</tr>
</tbody>
</table>

Table 2.2 Sample of commercial power GaN HEMTs for RF amplifiers.

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Output Power</th>
<th>Drain Voltage</th>
<th>PAE (%)</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TriQuint</td>
<td>63.1</td>
<td>40</td>
<td>55</td>
<td>3.5</td>
<td>15</td>
</tr>
<tr>
<td>Nitronex</td>
<td>182</td>
<td>28</td>
<td>63</td>
<td>0.9</td>
<td>18.3</td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>28</td>
<td>62</td>
<td>2.5</td>
<td>16</td>
</tr>
<tr>
<td>Eudyna</td>
<td>45</td>
<td>65</td>
<td>57.4</td>
<td>2.9</td>
<td>12</td>
</tr>
<tr>
<td>RFHIC</td>
<td>10</td>
<td>28</td>
<td>55</td>
<td>2.14</td>
<td>10</td>
</tr>
<tr>
<td>Cree</td>
<td>215</td>
<td>28</td>
<td>50</td>
<td>1.8 - 2.3</td>
<td>15</td>
</tr>
<tr>
<td>UMS</td>
<td>50</td>
<td>50</td>
<td>55</td>
<td>3</td>
<td>15</td>
</tr>
</tbody>
</table>

As previously stated, the output power could not exceed the level of 10 W/mm using the conventional configuration of HEMTs. By the introduction of the field plate metallization to the gate (called also overlapping gate) in GaN HEMT technology, as presented in Figure 2.1 [7], record values have been achieved. This field plate technology was first used in MESFET GaAs device in 1992; it has reached a breakdown voltage $V_{BD}$ of 42 V [13].

In AlGaN/GaN devices, the field plate metallization is implemented on the passivation layer (SiN). It reduces the critical peak gate-to-drain electric field distribution profile [14]. Special care should be considered due to its effect on operating frequency reduction, due to an increase in the gate-drain capacitance value. Consequently, the breakdown voltage has
been increased considerably, a breakdown voltage $V_{BD}$ of 1900V has been achieved in early 2006 [15]. Recently in 2008, a novel GaN array HFET configuration has reached 10400V and 3000V breakdown voltages with thick poly-AlN and SiN passivations, respectively [16]. In Table 2.1 a summary of up-to-date power AlGaN/GaN HEMTs for RF power amplifiers applications is given. Meanwhile, a sample of recently commercialized full-foundry released AlGaN/GaN RF power HEMT devices is presented in Table 2.2.

2.2 GaN Material Properties

To meet required specifications for high power amplifiers (HPAs), selected active devices material properties should be selected to have a direct impact on DC operation, RF output power, large-signal performances in terms of linearity and efficiency. The valuable properties in this regard, which give the highest figure of merit as presented at the bottom of Table 2.3, are bandgap energy, breakdown electric field, high sheet charge density (in HEMTs), thermal conductivity, electron and hole transport properties, saturated electron velocity and substrate conductivity. A resume of these semiconductor parameters is given in Table 2.3 for the commonly used semiconductor technologies [17] [18].

From data reported in Table 2.3, it is evident that GaN has the highest semiconductor material figure of merits for high power amplifier applications. Also, SiC is considered as the second most suitable material, the relatively low electron mobility and the lack of heterojunctions in SiC-MESFET confine its high frequency performance. For HPAs operation these parameters can be interpreted as follows:

- Wide bandgap energy (3.4 eV) and very high breakdown (critical) electric field (4 MV/cm) enable high internal electric fields (i.e. high terminals voltage); it is essential for high output power density. Consequently, recent GaN devices have achieved very high drain bias voltage ($V_{bias} = 135V$) [8]. On the other hand, this provides high input and output impedances and low parasitic output capacitance. They are key requirements for HPAs high linearity and efficiency by affording frequency independent broadband matching.

- The electron mobility (1500 to 2000 cm$^2$/Vs) and electron saturation velocity (2.1 x 10$^7$cm/s) enable high frequency performance. A current gain cutoff frequency $f_c$ more than 150 GHz
with a maximum oscillation frequency \( f_{\text{max}} \) more than 230 GHz for a gate length of 0.1 \( \mu \text{m} \) [19].

- The high sheet charge density of two-dimensional electron gas (2-DEG) in HEMT is fundamental for operation high current densities, with the contribution of the high saturation electron velocity [20].

- High thermal conductivity for both GaN (1.5 W/cmK) and SiC (4.9 W/cmK) is essential for high output power in HEMTs on SiC-substrate. GaN-based amplifiers can operate well at 300°C while silicon devices stop operating at 140°C [21].

- Relatively low dielectric constant (9.0) means low capacitive loading of a device. It reduces the parasitic time delay [22]. Also, it permits larger area devices with larger RF currents and RF output power for given impedance specifications [17].

### Table 2.3 Semiconductors material properties figure of merit [17] [18].

<table>
<thead>
<tr>
<th>Material Property</th>
<th>GaN</th>
<th>4H-SiC</th>
<th>GaAs</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap energy ( E_g ) (eV)</td>
<td>3.49</td>
<td>3.25</td>
<td>1.43</td>
<td>1.11</td>
</tr>
<tr>
<td>Breakdown electric field ( E_{br} ) 10⁶ V/cm</td>
<td>4.0</td>
<td>3.5</td>
<td>0.4</td>
<td>0.25</td>
</tr>
<tr>
<td>Saturated electric field ( E_{sat} ) 10⁵ V/cm</td>
<td>15</td>
<td>25</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>Electron mobility ( \mu^- ) (cm²/Vs)</td>
<td>2000</td>
<td>700</td>
<td>8500</td>
<td>1350</td>
</tr>
<tr>
<td>Hole mobility ( \mu^+ ) (cm²/Vs)</td>
<td>300</td>
<td>120</td>
<td>330</td>
<td>450</td>
</tr>
<tr>
<td>Saturation electron velocity ( v_{sat} ) 10⁷ cm/s</td>
<td>2.5</td>
<td>2.1</td>
<td>1.3</td>
<td>1.0</td>
</tr>
<tr>
<td>Maximum drift velocity ( \nu_d ) 10⁷ cm/s</td>
<td>3.0</td>
<td>2.0</td>
<td>2.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Thermal Conductivity ( \kappa ) (W/cmK)</td>
<td>1.5</td>
<td>4.9</td>
<td>0.56</td>
<td>1.5</td>
</tr>
<tr>
<td>Maximum temperature ( T ) (°C)</td>
<td>700</td>
<td>600</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Relative dielectric constant ( \varepsilon_r )</td>
<td>9.0</td>
<td>10</td>
<td>12.5</td>
<td>11.9</td>
</tr>
<tr>
<td>Baliga figure of merit (BFOM = ( e^*\mu^*Ebr^3 ))</td>
<td>24.6</td>
<td>3.1</td>
<td>9.6</td>
<td>1.0</td>
</tr>
<tr>
<td>Johnson figure of merit (JEM = ( E_{br}^<em>v_{sat}/2</em>\pi ))</td>
<td>80</td>
<td>60</td>
<td>3.5</td>
<td>1.0</td>
</tr>
</tbody>
</table>

A resume of semiconductor material properties as linked to enhanced device performances and communication system advantages is given in Table 2.4. Accordingly, GaN is considered as the ideal candidate for high power microwave devices [6] [23].
**Table 2.4** Wide bandgap material advantages for power amplifier applications [17][20].

<table>
<thead>
<tr>
<th>Material Property</th>
<th>Device Property</th>
<th>Improved Factor</th>
<th>System Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Wide bandgap</td>
<td>- High voltage</td>
<td>- Power density</td>
<td>- Less dies needed</td>
</tr>
<tr>
<td>- High critical field</td>
<td>- Low parasitic capacitance</td>
<td>- Power gain</td>
<td>- Less energy</td>
</tr>
<tr>
<td>- High thermal conductivity</td>
<td>- High temperature</td>
<td>- Efficiency</td>
<td>- High efficiency</td>
</tr>
<tr>
<td>- Wide bandgap SiC-substrate</td>
<td>- High output power</td>
<td>- High impedance</td>
<td>- Ease of matching</td>
</tr>
<tr>
<td>- HEMT Structure</td>
<td>- High frequency</td>
<td>- Thermal stability</td>
<td>- Smaller and cheaper package</td>
</tr>
<tr>
<td>- High electron velocity</td>
<td>- Low memory effect</td>
<td>- Larger power/die</td>
<td>- Reduced cooling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Smaller die size</td>
</tr>
</tbody>
</table>

2.3 AlGaN/GaN HEMT Operation Principle

In this section a brief description of the AlGaN/GaN HEMT basic operation and technology will be presented. As described in the previous section, the essential characteristic in the HEMT device is the formation of a free electrons layer at the channel. It is termed as the two dimensional electron gas region (2DEG), as shown in Figure 2.2. It is created in the GaN layer side at the AlGaN/GaN heterojunction interface between the wide (AlGaN: 3.95 eV) and narrow (GaN: 3.4 eV) bandgap energies, respectively. The Fermi energy of this thin layer is above the conduction band thereby creating a sheet of free electrons, which makes the channel highly conductive.
Figure 2.2 Basic structure of AlGaN/GaN HEMT and related conduction band diagram depicting the 2DEG formation.

In Figure 2.2, the Si doped AlGaN is grown on top of the GaN material. A key feature of the nitride based active devices is the presence of a strong polarization field within the crystal. The AlGaN/GaN crystal is constructed in a way that the total polarization field adds [24]. The Si impurities donate free electrons, which under the presence of this polarization form the two-dimensional electron gas (2DEG) [20]. The generated 2DEG have high mobility as electrons are physically separated from the source scattering impurities (ionized Si donors in AlGaN layer). This characteristic is unique for HEMT active devices.

Furthermore, in contrast to GaAs HEMTs, AlGaN/GaN 2-DEG can be obtained without any doping due to the available large polarization effect [24]. In the following, the two distinct types of polarization in AlGaN/GaN HEMTs, spontaneous and piezoelectric polarizations, are presented.

2.3.1 Piezoelectric Polarization

The HEMT polarization electric field is mainly dependent on AlGaN/GaN crystalline growth face (Ga-face or N-face), AlGaN thickness, and increased aluminum content in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer. It is the sum of the piezoelectric polarization field of AlGaN layer and the resulting spontaneous polarization field of AlGaN/GaN layers, respectively. Figure 2.3 illustrates a schematic of the crystal structure grown of GaN layer, Ga-face (0001) and N-face (0001), respectively. Most AlGaN/GaN HEMTs are
grown on Ga-face (0001). It produces uniform and flat interfaces with high quality heterostructure [24].

The piezoelectric polarization (\(P_{PE}\)) is induced by the distortion of the crystal lattice due to the lattice constant difference between AlGaN and GaN materials. It results from the tensile stress caused by the growth of the strained Al\(_x\)Ga\(_{1-x}\)N on GaN (Ga-face). Due to the large value of the present piezoelectric effect, a large sheet of charges results at both faces of AlGaN layer, as presented in Figure 2.4(a).

**Figure 2.3** Schematic of the crystal structure of the growth orientation, Ga-face and N-face GaN crystal. Adopted from [24].

**Figure 2.4** Polarization electric field for a strained AlGaN crystal grown on relaxed GaN crystal (Ga-face crystal growth), (a) large piezoelectric electric field induced charge sheet in strained AlGaN, (b) spontaneous electric field induced charge sheet present in both GaN and AlGaN crystals.
2.3.2 Spontaneous Polarization

The spontaneous polarization ($P_{SP}$) for GaN and AlN are pointing towards the substrate for Ga-face heterostructures. It results from the built-in static electric field in an unstrained crystal. It appears when the crystal lacks inversion symmetry and the bond between two atoms is not purely covalent. The electron charge cloud shifts towards one atom along the direction in which the crystal lacks inversion symmetry. The net positive charge is shifted to one face of the crystal, and a net negative charge is created in opposite face. In Figure 2.4(b), an illustration of the spontaneous polarized electric fields and equivalent induced sheet charges are present for GaN and AlGaN crystals (Ga-face crystal growth).

The piezoelectric in the strained AlGaN layer and spontaneous polarization in AlGaN/GaN have the same orientation (i.e. Ga-face crystal growth orientation). Since polarization field in the AlGaN layer is higher than the GaN buffer layer, the presence of a polarization field discontinuity at the AlGaN/GaN interface will induce a very high positive sheet charge. This charge is the resulting 2DEG charge ($\sigma$), and is proportional to the total polarization across the AlGaN/GaN interface. Figure 2.5 and Figure 2.6 illustrate the 2DEG sheet carrier density as function of AlGaN layer thickness and aluminum mole fraction ($x$), respectively [25]. Its charge density is considerably high ($n_s \sim 2 \times 10^{13}$ cm$^{-2}$), approximately 10 times GaAs HEMT. This enables GaN HEMTs to reach record peak currents of more than 1 A/mm. Also, as the channel resistance at low electric field is inversely proportional to charge density $n_s$, very low turn-on resistances are reached.

2.4 Trapping Mechanisms and Current Collapse

Despite the excellent technology properties of AlGaN/GaN HEMT devices, one of the main problems is to reduce drain current collapse. It is mainly related to imperfections and impurities in active region, which give rise to charge trapping. These imperfections can trap and release sufficient quantity of electrons to alter $I(V)$ characteristics. The charge trapping and de-trapping is a slow process with characteristic time constants in the range of microseconds [26]. It causes voltage delay in the device operation and restricts fast drain-current and voltage excursions in HEMTs RF output power, as will be detailed in Chapter 5. In the following, the dominant trapping mechanisms in HEMTs are presented, as illustrated in Figure 2.7.
Figure 2.5 Dependence of the 2DEG sheet density on AlGaN layer thickness, experimental data (marker), least-square linear fit (solid line). Adopted from [25].

Figure 2.6 Dependence of the 2DEG sheet density on Al mole fraction ($x$) in Al$_x$Ga$_{1-x}$N compound material, experimental data (marker), least-square linear fit (thin solid line), and with barrier height of 1.42V (dotted line). Adopted from [25].
Figure 2.7 AlGaN/GaN HEMT structure illustrating polarization, trapping mechanisms (surface, buffer), and buffer current conduction with their impact on 2DEG electrons.

2.4.1 Surface States (Surface Traps)

As AlGaN layer thickness is increased during the growth process, total polarization electric field increases accordingly. Above a limit thickness (known as critical thickness) the internal electric field becomes high enough to ionize donor states at the surface causing electrons to drift towards the AlGaN/GaN interface. As the electrons move from the surface to the interface, the polarization electric field gets weaker till it reaches equilibrium with zero electron transfer. At this stage, the 2DEG is formed by the transferred electrons, and positive surface states are formed from the Si ionized donors. Therefore, the higher surface states are, the larger the 2DEG channel region charge density is [24].

In terms of energy levels, the 2DEG cannot be formed unless AlGaN layer is thick enough to allow the valence band to reach the Fermi level at the surface. Electrons can then transfer from AlGaN valence band to the GaN conduction band, leaving behind surface holes (i.e. surface positive sheet charge). This means that in all cases, a positive sheet charge at the surface must exist in order for the 2DEG to be present in the AlGaN/GaN interface.
Therefore, surface states, located in the access regions between the metal contacts, act as electron traps. A technology key parameter in HEMTs is surface passivation process; it must avoid the positive surface states (charges) from being neutralized by trapped electrons. In reality, passivation process is still imperfect. The electrons from the gate metal can be trapped under large electric field present during large-signal operation [27]. This reduces surface charges which induces a decrease in the 2DEG channel current. Corresponding drain current collapse in under RF operation is called surface trapping current dispersion, which will be characterized with time constants in details in Chapter 5.

2.4.2 Buffer States (Deep Traps)

Buffer traps, also called deep traps, are located deep at the interface between the buffer layer and the substrate. Under high drain-source voltage, electrons in the 2DEG channel could be captured by the buffer traps. The trapped electrons produce a negative charge, which depletes the 2DEG, and therefore decreases the channel current [27]. This reduction in the current under RF operation is called buffer traps current dispersion, which will be covered in details with time constants in Chapter 5.

Deep traps are primarily linked to the large lattice mismatch between the GaN and the substrate, which creates a large number of threading dislocation in GaN layer. These threading defects manifest themselves as deep electron traps. To reduce this type of deep traps, a relaxation (transition) layer is added between GaN buffer and substrate [28].

Another source of deep traps is the buffer compensation process to obtain high insulating material. Availability of background electron concentration in the buffer material due to native shallow donors cannot be avoided. These donors are compensated by adding deep acceptors. In under-compensation, a parasitic leakage current is induced through the buffer close to the substrate. This current deteriorates the pinch-off characteristic of the device. Meanwhile, in over-compensation, excess deep acceptors will behave as electron traps. Therefore, a key technology solution for this type of traps is the optimization of the compensation process [29].
As shown in section 2.2, another important factor in drain current collapse is self-heating in large-gate periphery AlGaN/GaN HEMTs due to large channel current conduction. A close analysis of the HEMT device behavior shows that its electrical behavior is highly correlated to channel temperature variation. Physical quantities such as bandgap energy, band offset energy, drift velocity, electron mobility, and the free electron carrier density are all temperature dependent. As an example for high power operation, it has been shown as temperature increases the electron mobility decreases, as given in Figure 2.8(a) [30]. Also, as presented in Figure 2.8(b) [31], a decrease in drift velocity due to decreased saturation electric field is apparent, thereby the drain current collapses affecting HEMT DC and RF performances. Any fluctuation in ambient temperature or any variation in DC or RF power dissipation brings a change in channel temperature; in its turn affects the channel drain current. The drain current variation subject to self-heating effect is known as drain current thermal dispersion. In large-signal HPAs, this self-heating effect introduces distortion in output RF signal, which is known as thermal memory distortion effect. It introduces an unavoidable nonlinearity in RF signal dynamics the proposed electrothermal large-signal model should predict. More discussions about static and dynamic thermal effects on drain current will be presented in next chapters.

Figure 2.8 AlGaN/GaN HEMT physical quantities dependency on channel temperature, (a) electron mobility with different Al-mole fraction, (b) electron velocity versus applied electric field. (a) and (b) adopted from [30] and [31], respectively.
2.6 AlGaN/GaN HEMT Technology Issues

The AlGaN/GaN typical HEMT topology is presented in Figure 2.9. The layers structure is generally composed of substrate layer, the nucleation layer, buffer, spacer, carrier supply, barrier, and cap layers. The main improvements, technology related issues, and refinements to improve device performance such as drain current collapse, transconductance, gain, and gate leakage current will be summarized in the following sub-sections starting from the substrate to the HEMT electrodes level.

![Figure 2.9 AlGaN/GaN HEMT on SiC structure topology [32].](image)

2.6.1 Substrate

The substrate is an important factor regarding RF performance and cost of AlGaN/GaN HEMTs fabrication. Generally, three types of substrates are available, silicon carbide (SiC), sapphire (Al$_2$O$_3$) or silicon (Si) substrates. The appropriate choice for RF HPAs is SiC despite its cost and difficulty to grow in large wafer size for mass production (4-in available versus 12-in for Si). The use of SiC semi-insulating substrate is mostly due to its high thermal conductivity and high resistivity with the lowest lattice and thermal expansion mismatch to GaN layer. Recently, new low-cost substrates have been introduced by Cree Company; it has improved the epitaxial quality and reduced dislocations densities [33].
2.6.2 Epitaxy

As illustrated in Figure 2.9, the epitaxy is the set of layers between the SiC substrate and the gate metallization electrode. Each layer related HPAs performances and technology challenges will be briefly described.

- **Nucleation Layer**
  
The thermal expansion and crystalline structural mismatches between SiC and GaN induce substantial levels of tension in the GaN-SiC interface. A key challenge in HEMT is to grow an adequate interface transition material between the GaN and SiC. The interface material must be capable of absorbing and dissipating the available tension. Materials such as AlGaN and AlN are used in recent process technologies to reduce interface mismatch, defects and trapping formation which result in decreased current collapse at described previously [18].

- **Buffer layer**
  
A relatively thick undoped semi-insulating GaN layer is used for the 2DEG formation at the upper interface, as described in section 2.3. Also, it serves as insulator to lower background carrier concentration and therefore reducing drain current collapse by reducing buffer trapping effect.

- **Spacer Layer**
  
The AlGaN spacer layer is used to separate the hetero-interface from the doped Si-donor AlGaN layer to ensure high carrier mobility and density. The thickness of the spacer layer is essential and critical for HEMT performance. Its increase avoids ionization scattering from dopants which increases electron mobility, meanwhile the channel carrier concentration decreases due to difficulty for electrons to reach the channel [34].

- **Carrier Supply Layer**
  
In intentionally doped HEMTs, AlGaN (Si-donors) supply layer is used for enhancing 2DEG carrier density. The contribution of this doping affects the 2DEG density by 20% at most, since the 2DEG density is formed initially by the large polarization field [29]. Furthermore, high modulation-doped devices have shown improved DC performance, but degraded RF performance due to reduced electron saturation velocity as compared to undoped devices [35].
 Barrier Layer

It assures the barrier height of the gate Schottky contact. Its thickness is application dependent, a trade-off between less saturated RF power (thinner layer) and small-signal RF gain (thicker layer) [36].

Cap Layer and Leakage Current Problem

An n-type doped cap-layer GaN is used to maintain the polarization-induced surface charges, which reduces drain current collapse [37]. It enhances source and drain ohmic contacts, and improves breakdown voltage. Furthermore, it reduces leakage current problem at high input RF signal, which is a real challenge in HPAs. Recent HEMT technologies address this problem by introducing insulating dielectric layers such as SiO$_2$ and Si$_3$N$_4$ to form MOSHFET and MIS-HEMT, respectively. Both reverse leakage and gate-forward currents were suppressed using metal-insulator-semiconductor gate structure [38] [39].

2.6.3 Access Region

The access region and related technology structure topology issues will be described in the next points with conjunction to HPAs performances.

Ohmic and Schottky Contact

Source and drain ohmic contacts using Ti/Al, Ti/Al/Ti/Au/WSiN or Ti/Al/Ni/Au are used. Recessed ohmic technique is also used to reduce the ohmic contact resistance. The Schottky gate contact is usually made from Ni/Au or Pt/Au. The gate metallization is closer to the source than the drain to avoid premature breakdown. An air-bridge technology using an electroplated Au is used to connect the source pads of multifinger HEMT structures [32].

Surface Passivation

Drain current collapse due to surface trapping and knee-voltage increase problems have been largely solved by surface passivation (SiN). However, it introduced a drawback in breakdown voltage, which has been recovered by adding field-plate structures, as illustrated in Figure 2.1. Recently, AlN has been used; very high breakdown voltages has been achieved [16].
Field Plate Technology

First developed gate field plate type (G-FP) covers the gate and extends to the access region on the gate-drain side. Its role is reducing peak-electric field on the gate to drain-side edge. Its drawback is increased gate-drain feedback capacitance at low voltages and extended depletion length at high voltage, which results in gain drop. A trade-off between gain and breakdown voltage defines field-plate length. To solve this issue, source field plate (S-FP) was developed, which reduces feedback capacitance \( (C_{gd}) \) and improves large-signal gain \([40]\). Moreover, FP related capacitance is absorbed in output-matching network. Also, the large-signal input voltage swing dynamic does not modulate the FP induced depletion region; this improves device linearity issue. Another type is field-plate with recessed-gate structures. It enhances channel separation from surface traps at high drain voltages. It improves transconductance, gain and also helps to reduce leakage current \([41]\).

Novel technological issues are still under investigation to meet the broad range applications of AlGaN/GaN HEMTs. Technical task such as power switching, normally-off operation desired for safety operation, is under focus. GaN HEMTs are able to cut power in standby mode and achieve over 100W output power. This enables the attractive inherent low on-state resistance and high breakdown voltage usage in RF power switching amplifiers \([16]\). All above stated issues have an important effect on HPAs I(V) characteristics. Therefore, any small- or large-signal characterization procedure and modeling strategy should account for any induced dispersion and predict any type of distortion, as will be discussed in details in the following chapters.

References


Chapter 3

AlGaN/GaN HEMT Thermal Modeling and Analysis

As previously discussed, one of the key factors for AlGaN/GaN technology is its relatively high temperature operating level. This reduces the current flow in the channel, increases the knee voltage, and introduces self-heating memory effect in total drain-source current. To enhance the model capability to predict and simulate this response correctly in CAD environment, thermal models are needed in large-signal model implementation for AlGaN/GaN HEMT devices.

Therefore, in this chapter, a detailed discussion of the HEMT thermal model extraction and implementation is covered. First, numerical analysis is handled for the device structure to have a total thermal profile. From steady state thermal modeling, the thermal model resistances are extracted for the multilayered HEMT structure. Followed by the transient thermal analysis of the structure, the thermal model capacitances are extracted depending on the order of the thermal model proposed. This increase in order helps in capturing static and dynamic thermal variations due to static and RF excitation in real power HEMTs for RF applications.

3.1 HEMT Thermal Model Formulation Fundamentals

In this part, the thermal model equivalent circuit topology and principle is covered. From the physics of heat transfer, in semiconductors technology, the dominant heat transfer mechanism is through conduction towards the SiC substrate or the case heat-sink of the AlGaN/GaN HEMT. This conduction mechanism is mainly related to the atomic (crystalline)
activity in the material. The heat transfer takes place from high energy elements to lower energy ones. In semiconductor materials, this heat transfer conduction happens on the form of lattice (crystalline) vibration.

### 3.1.1 Thermal Resistance Definition

The thermal resistance is, by definition, the characteristic by which the material is opposing heat dissipation and heat conduction. The smaller is the thermal resistance value, the smaller is the change in temperature due to high thermal conductivity, and higher thermal resistance values leads to large increase in temperature.

\[
\Phi = -\kappa(T) \cdot \nabla T
\]

where \( T \) is the temperature in degree Kelvin (K) and \( \kappa(T) \) is the temperature dependent thermal conductivity of the medium given in [W/(m·K)]. By integrating the heat flux distribution in (3.1) over the surface of incidence, we obtain for a constant power dissipation \( P_{\text{diss}}(W) \) the steady state solution as

\[
P_{\text{diss}} = \frac{\Delta T}{R_{\text{th}}}
\]
where the resulting factor $R_{th}$ ($\degree C/W$) is defined as the thermal resistance of the homogeneous medium. It reflects the medium response to heat transfer mechanisms. It includes all the medium thermal parameters (thermal conductivity, thickness, and thermal boundary conditions). This steady state thermal expression can be used for any semiconductor device to calculate the HEMT device channel average temperature $T_{ch}$ for a given power dissipation $P_{diss}$ and an initial temperature reference $T_0$ (ambient temperature). The resulting linear relationship between the channel temperature and average dissipated power in static DC is obtained as [1]

$$T_{ch} = R_{th}P_{diss} + T_0$$

(3.3)

where $R_{th}$ ($\degree C/W$) is the equivalent thermal resistance of the HEMT device structure and $T_0$ is the ambient temperature. And the average dissipated power can be determined for the HEMT device by its quiescent bias conditions ($V_{DS0}, I_{DS0}$),

$$P_{diss} = V_{DS0}I_{DS0}$$

(3.4)

### 3.1.2 Thermal Capacitance Definition

Similarly, a more general form of (3.2) can be obtained for a time varying thermal analysis in semiconductor devices subjected to instantaneous time dependent power dissipation $P_{diss}(t)$. The resulting expression for above development in time domain can be reduced to [2]

$$P_{diss}(t) = \frac{\Delta T_{ch}}{R_{th}} + C_{th} \frac{d}{dt}(\Delta T_{ch})$$

(3.5)

The first term in (3.5) reflects the conductive heat generation as function of channel temperature and thermal resistance, as previously explained. The second term in (3.5) reflects the dynamic heat flow due to the heat stored in the semiconductor material. Since this characteristic is directly related to the ability of the semiconductor material to store heat (defined as heat capacity in materials), the resulting coefficient $C_{th}$ is defined as the thermal capacitance of the semiconductor material. Therefore, the total instantaneous power dissipation generated heat ($P_{diss}(t)$) is the sum of heat flow term ($\Delta T_{ch}/R_{th}$) and heat storage term ($C_{th} [d(\Delta T_{ch})/dt]$).
3.1.3 Thermal Model Implementation in CAD

By determining the thermal resistance presented in the thermal capacitance described in (3.5), a thermal model representation in large-signal modeling is possible in CAD. To predict the temperature change and its corresponding drain current variation in the HEMT device channel, an equivalent electrical circuit is used. By analogy to electrical circuits, replacing the instantaneous power dissipation \( P_{\text{diss}}(t) \) and the channel temperature \( T_{\text{ch}} \) in (3.5) by a current source \( I_{\text{th}}(t) \) and a potential difference \( V_{\text{th}}(t) \), respectively, (3.5) reduces to

\[
I_{\text{th}}(t) = \frac{\Delta V_{\text{th}}}{R_{\text{th}}} + C_{\text{th}} \frac{d}{dt}(\Delta V_{\text{th}})
\]  

This equation clearly shows the sum of two currents under the same potential difference \( \Delta V_{\text{th}} \). The first term is the conductive current across the thermal resistance \( R_{\text{th}} \) and the second term is the displacement current across the thermal capacity \( C_{\text{th}} \). Therefore, a parallel \( R_{\text{th}}C_{\text{th}} \) filter is the electrical equivalent circuit that can be used to simulate the thermal response of the semiconductor device. Figure 3.2(a) shows the first-order thermal equivalent model implementation in CAD environment. Similar formulation can be extracted in complex notation. The instantaneous power dissipation is replaced by the complex current notation given by

\[
I_{\text{th}}(\omega) = P_{\text{diss}}(\omega) = v_{ds}(\omega) \cdot i_{ds}(\omega)
\]  

The resulting channel temperature difference \( \Delta T_{\text{ch}} = T_{\text{ch}} - T_0 \) is equivalent to the simulated voltage across the thermal model terminals given by

\[
\Delta T_{\text{ch}}(\omega) = \Delta V_{\text{ch}}(\omega) = H(\omega) R_{\text{th}} I_{\text{th}}(\omega)
\]  

where

\[
H(\omega) = \frac{1}{1 + j\omega R_{\text{th}}C_{\text{th}}}
\]  

represents the first-order low-pass filter transfer function of the thermal model. Depending on the thermal model extraction method, as will be presented in the next sections, higher-order low-pass filter can be used. In Figure 3.2(b) a third-order low-pass filter sub-circuit thermal model
representation is shown. In ADS® software, the thermal model sub-circuit under instantaneous power dissipation calculates the channel temperature for the nonlinear drain current expression. An iterative process is established between channel temperature estimation and drain current evaluation till the solution converges.

Figure 3.2 Thermal model equivalent sub-circuit representation in large-signal model of AlGaN/GaN HEMTs to determine channel temperature, (a) First-order low pass filter representation, (b) Third-order low-pass filter representation for increased accuracy.

In the next section, AlGaN/GaN HEMT structure thermal analysis and simulations is handled in order to get a deep understanding about the thermal profile as a function of conductivities, thermal boundaries, physical, and geometrical parameters changes for further use in thermal model implementation.

### 3.2 Thermal Analysis of AlGaN/GaN HEMT Structure

For power dissipation due to drain current conduction in the 2DEG active region, a heat transfer procedure described by the heat transfer equation, given by [3]

$$\nabla \cdot (\kappa(T) \nabla T) - \rho_m C_p \frac{\delta T}{\delta t} = -H \quad (3.10)$$
can be evaluated to obtain the thermal profile of the AlGaN/GaN HEMT structure and the channel temperature. $T$ is the temperature in Kelvin (K). $\kappa(T)$ is the temperature dependent thermal conductivity of the given layer in (W/m·K); it depicts the thermal conduction heat transfer rate to boundaries and surrounding environment. $H$ is the dissipated power density (heat generation term) in (W/m$^3$); it quantifies the generated heat rate of change in the material. $\rho_m$ is the mass density in (kg/m$^3$). $C_p$ is the heat capacity given in (J/kg·K) for each layer; it reflects the material capacity to store some of the heat energy by rising its temperature. The heat equation is implemented taking into account all types of heat transfer mechanisms and boundary conditions of the device. All of the conductive, convective, and radiative terms, are represented in the heat generation term ($H$) of the heat equation using the energy conservation principle. By solving (3.10), the layers temperature distributions, the HEMT’s hot spots, the thermal resistance of each layer, the heat storage, and the thermal boundaries discontinuities can be obtained.

### 3.2.1 Thermal Conductivity Degradation in HEMTs

One more important parameter, to be considered, is the thermal conductivity of materials constituting the HEMT device [4]. This term is to be investigated delicately due to its high effect on device temperature. In all references, it has been shown that it is temperature dependent. It decreases with increasing temperature for the AlGaN/GaN materials, as illustrated in Figure 3.3 (adopted from [5]).

In thermal modeling of semiconductors using analytical techniques or closed form expressions, the nonlinear heat equation and thermal conductivity, represented by (3.10) and (3.11), respectively, are converted to linear ones using Kirchhoff’s transformation [5] [6]. There are several expressions to describe the thermal conductivities of semiconductor materials. The one used here to depict its variation with temperature is given as [7] [8]

$$\kappa(T) = \kappa_i \left(\frac{T}{T_0}\right)^{-\alpha_i} \quad (3.11)$$

where $\kappa_i$ is the thermal conductivity at room temperature ($T_0 = 300K$) for the semiconductor material. Published data are $\kappa_{GaN} = 1.6 \text{ (W/cm·K)}$ and $\alpha_{GaN} = 1.4$ for GaN and $\kappa_{SiC} = 3.3 \text{ (W/cm·K)}$ and $\alpha_{SiC} = 1.5$ for SiC.
3.2.2 AlGaN/GaN HEMT Structure

The HEMT structure of devices under consideration is illustrated in Figure 2.9. A simplified structure is used for thermal investigation formed of the back plate heat-sink (Au/Sn), the semi-insulating substrate layer (4H-SiC), buffer layer (GaN), and barrier layer (AlGaN) as shown in Figure 3.4 [9].

![Figure 3.4 AlGaN/GaN HEMT structure of the transistor investigated in this work [9], simulated layers (Sn/Au/SiC/GaN/AlGaN).](image)

**Figure 3.3** GaN epitaxial layers and SiC substrate thermal conductivity degradation with temperature in AlGaN/GaN HEMTs [5].
A simpler structure can be used in analytical techniques or closed-form approximations. The most relevant layers for thermal impedance determination are the SiC substrate layer and the heat-sink related material [10].

3.2.3 HEMT Structure Thermal Profile Simulations

The heat equation described above in (3.10) is solved using numerical finite element method. The physical quantities are introduced over the domain of integration of the AlGaN/GaN HEMT structure as described by Figure 3.4. The estimated total dissipated power is partitioned on the HEMT distinct fingers. A power density distribution (W/m²) is calculated and determined for each finger. This power distribution has been implemented in the software as a thermal Dirichlet boundary condition via the heat generation term in the heat equation. The processed solution of the finite element formulation is given by

\[
[M]\dot{T} + [K]T = H
\]

(3.12)

where, \(T\) and \(\dot{T}\) and are the steady state temperature profile generated by an average static power dissipation and the time-dependent temperature profile generated by a transient (dynamic) power dissipation of the complete structure, respectively. \(M\) (°C/W) is related to the heat capacity and the mass density; it is called the mass matrix. \(K\) (°C/W) is the conductivity related coefficient matrix; it is called the stiffness matrix. Equation (3.12) provides a discrete system formulation of the complete HEMT structure temperature. It includes the static and the dynamic thermal profile of the complete meshed HEMT structure.

A reference temperature of \(T_0 = 300\text{K}\) is imposed on the structure and substrate base (heat-sink case for on-wafer or packaged devices). This reference temperature serves as initial boundary condition on all the HEMT boundaries. Thermal Dirichlet boundary condition is used for the case heat-sink or the base temperature to be equivalent to the fixed chuck temperature controller. Another used boundary is the thermal Neumann boundary condition. It is used to represent the incident normal heat flux through the HEMT structure limits and artificial symmetry boundary condition.
Simplified structure has been used for the simulation of the multi-finger HEMT device, as shown in Figure 3.4. In the real HEMT structure, used in this work for the 3.2-mm HEMT, a heat-sink layer is used to consider the effect of the transistor case based on data from reference [9].

Due to symmetry, half of the HEMT structure is simulated to reduce space and time numerical complexities. As shown in Figure 3.5, the simulated thermal profile of the HEMT structure shows clearly the hot spots in the gates fingers area, which is higher at the central finger to the right and lower at the lateral finger to the left; lateral fingers show less increase due to heat dissipation to lateral edges. Inset shows a larger view of the hotspots fingers area. The displayed temperature is given as the difference between the calculated temperature and the reference temperature $T_0 = 300K$. Similarly, the non-uniform temperature distribution is made apparent in Figure 3.6, the inner fingers suffer from excessive heat dissipation as compared to the lateral fingers, which proves that the contribution of individual fingers to drain current is not equal; the lateral fingers contribution is higher than the middle ones.

Using this numerical approach, the nonlinear thermal conductivities dependency on temperature variation, given in (3.11) of the semiconductor layers of the HEMT structures, is taken into account. For large difference in two adjacent layers thermal conductivities, a large thermal boundary resistance discontinuity rises (thermal mismatch). This particular problem cannot be solved in closed form expression [11]-[13], whereas in this approach this effect is identified and thermal boundary discontinuity is included. It is found that the GaN/SiC interface thermal boundary resistance strongly influences the temperature rise in the AlGaN/GaN device channel [14].

To show this discontinuity, thermal mismatch is presented in Figure 3.7 (not to scale) at layers interfaces with AlGaN/GaN/SiC nonlinear temperature dependent thermal conductivities. The thermal discontinuities are apparent by calculating the temperature gradient over the simulated structure. A realistic HEMT structure is shown in Figure 3.8 in the channel fingers area. The discontinuity is clearly shown even for relatively low self-heating temperature.
Figure 3.5 A two-dimensional cross-sectional area of the thermal profile of an 8-finger structure (8 x 400 µm HEMT), the 4 hot spots represent the 4 left fingers of the simulated HEMT structure.

Figure 3.6 Non-uniform thermal distribution of the 3.2-mm (8 x 400 µm) HEMT. The temperature gradient is higher at the channel under the gate in the middle fingers as compared to the lateral fingers.
Figure 3.7 Thermal mismatch at layers interfaces due to difference in the nonlinear temperature dependency of thermal conductivities of adjacent layers (not real scale), thermal mismatch is made apparent by calculating the gradient of temperature.

Figure 3.8 Thermal mismatch shown at the interface between GaN/SiC for a realistic HEMT structure by evaluating the temperature gradient. Layers have nonlinear temperature dependent thermal conductivities.
In the next section, two main points will be presented. First, the complete study of the steady state heat transfer in the AlGaN/GaN HEMT due to static DC power dissipation is handled. Then, the HEMT structure thermal resistance is extracted from steady state thermal simulation, which is used in the thermal equivalent model.

### 3.3 Steady-State Simulation and Thermal Resistance Estimation

After the evaluation of the steady-state thermal profile, as described in the previous section for the 3.2-mm AlGaN/GaN HEMT, the non-uniform distribution of the temperature is obtained under each finger of the HEMT. By determining the temperature change for each finger under the introduced power dissipation, thermal resistance for each finger is extracted separately. The total thermal resistance of the 3.2-mm HEMT is calculated by means of the thermal resistance of individual fingers using averaging or integration over the entire finger area.

For device technology, temperature increase information is very important for the whole structure. Analysis and study of the temperature at interfaces between adjacent layers and at heat-sink are the most focused. It affects directly the nonlinear drain current in the 2DEG channel. This development helps to extract from the temperature profile the channel-to-gate surface temperature and the SiC/GaN layers interface temperatures, from which the thermal resistance can be defined for any layer and at any point of the HEMT structure. Figure 3.9 shows the temperature distribution at the 2DEG channel level for the complete HEMT device, the maximum temperature is at the central finger to the right and decreasing to the lateral finger to the edge of the devices. In Figure 3.10, for the same static power dissipation, the temperature distribution is given for all points at the interface between the SiC substrate and the GaN buffer layer (Figure 3.4). A difference in temperature of approximately 90°C is noticed at the position under the central finger as compared to the channel level.

Temperature distribution between the different layers in the HEMT structure (such as Figure 3.9 and Figure 3.10 for AlGaN/GaN and SiC/GaN, respectively) can be used directly in evaluating the thermal resistance of each layer separately by dividing the temperature difference by the dissipated power. The thermal resistances of the 8 individual fingers, illustrated in Figure 3.11, are extracted at the channel under the gates of the
8 fingers. In case the modeling strategy is based on unit transistor model for one finger cell or scaled transistor model, these thermal resistances are attributed to the first-order thermal model resistance of each of the eight cells in order. The drain current contribution of each model will be different from one model to the other.

Figure 3.9 Temperature profile at the interface between the AlGaN barrier layer and the GaN buffer layer (AlGaN/GaN) at the 2DEG channel level under the fingers for the 3.2-mm (8 x 400 µm) HEMT device, (P_{diss} = 20W, T_{ref} = 300K).

Figure 3.10 Temperature profile at the interface between the SiC substrate and the GaN buffer layer (GaN/SiC) for the 3.2-mm (8 x 400 µm) HEMT device, (P_{diss} = 20W, T_{ref} = 300K).
In our case, the model implementation will be for one 3.2-mm HEMT device, therefore, the total thermal resistance is evaluated from these 8 parallel finger’s individual thermal resistances [15].

Figure 3.11 Equivalent thermal resistance for each individual finger in the 3.2-mm HEMT device with 10 W total dissipated power, on-wafer package considered (Sn, Au) [9].

In Figure 3.12 the thermal resistance of an on-wafer structure (with packaging solder layer (Sn) and gold back-case (Au)) is presented as a function of the total dissipated power. As the power dissipation increases, the temperature increases, which degrades the nonlinear thermal conductivities of the HEMT device materials. This introduces an increase in the total thermal resistance of the GaN HEMT structure.

Figure 3.12 Total thermal resistance of the 3.2-mm HEMT device as function of dissipated power density (with packaging Au, Sn).
In the next section, two main points will be presented. First, the transient thermal simulation related to the transient (pulsed time-dependent signals) power dissipation will be covered for the HEMT structure fingers. Then, the transient thermal time constants of the HEMT structure are calculated. These time constants will determine the thermal capacitances of the proposed thermal model in Figure 3.2.

3.4 Transient Thermal Simulation and Time Constant Derivation

In this part, the main idea is to determine the thermal response of the AlGaN/GaN HEMT device in the presence of transient DC power dissipation, from which the thermal time constant can be deduced for individual fingers and for total structure. This thermal time constant is used in the thermal model implementation of the look-up table-based electrical model. Moreover, this procedure helps us in enhancing the thermal model through the knowledge of the transient behavior for individual layers and fingers, by inserting multi-time constants in thermal model topology [16].

Simulated transient response data and corresponding first-order curve fitting are presented in Figure 3.13(a) for individual fingers in 8 x 400 µm AlGaN/GaN HEMT device. The obtained results show an exponential trend. The first-order exponential curve fitting approximation for the resulting simulated transient thermal profile gives time constants of 83.44 µs, 83.60 µs, 85.26 µs and 91.80 µs for the four fingers from central to lateral finger, respectively.

Analyzing data for the central finger transient thermal temperature, as illustrated in Figure 3.13(b), we noticed that the temperature rise is relatively very slow above 1 µs. It is very fast below 1 µs as presented in the inset figure. Consequently, this fast variation cannot be described at the thermal circuit modeling level by a simple first-order RC thermal model implementation commonly used for slow thermal time constant. Therefore, multiple time constants representation should be used in the thermal model circuit implementation. This will lead to higher-order RC thermal model as presented in Figure 3.2(b).
Figure 3.13 Transient simulated temperature and exponential curve fitting for 3.2-mm HEMT structure: (a) the channel under individual fingers (four fingers are shown), (b) 2nd order fitting for the central finger and inset shows fast transient at 1µs range. Curve fitting represented by solid lines and simulations by symbols.

A second-order exponential curve fitting is given for the central finger in the 3.2-mm HEMT in Figure 3.13(b). It accurately approximates the simulated data. The resulting time constants are 23.71 ns and 87.51 µs for fast and slow transient thermal temperatures, respectively. This second-order approximation can be considered more realistic than the first-order approximation of the thermal behavior of the AlGaN/GaN HEMT device. The fast and slow transient thermal variations reflect the epitaxy and SiC layers transient thermal variation, respectively.
Figure 3.14 Transient thermal profile depicting fast and saturation variations for 3.2-mm HEMT (a) at the SiC substrate interface to AlGaN layer, (b) at the surface under the gate fingers (channel temperature). Δt = 50 µs.

To depict more the epitaxial and SiC layers transient thermal behavior, Figure 3.14 is shown. The curves are taken at time intervals Δt = 50 µs. It can be used to extract the second-order curve fitting approximation of the transient temperature of the GaN HEMT device. The two curves describe the dominant heat conduction factors in the AlGaN/GaN HEMT device. From Figure 3.14(a), the saturation temperatures of the SiC substrate under the fingers levels can be determined; under the central finger level it is 34 °C to reference...
temperature. In Figure 3.14(b), the temperature rise on the central finger (total temperature in the central finger) is found equal to 58.89 °C. Comparing with the second-order curve fitting, using developed Matlab fitting routines, we noticed that the two extracted slow and fast thermal time constants match approximately the transient temperature of SiC layer and epitaxial layer, respectively. The corresponding thermal resistances are obtained through calculation of the ratio of saturation temperature rise in each layer to dissipated power. The thermal capacitances for each layer are the ratio of time constants to calculated thermal resistances.

This leads us to an enhanced implementation of the thermal model using higher-order RC thermal model that describes the HEMT thermal profile more accurately than the first-order RC model. The thermal resistance is obtained through the calculation of the ratio of the temperature rise in each layer to the dissipated power (for individual fingers or total HEMT structure). The thermal capacitances are just the ratio of the time constants to the thermal resistances. For scaling tasks in large-signal electrothermal modeling, this is a powerful tool. First the thermal model is developed with the large-signal model for the unit-cell transistor. Then using above procedure for large number of gate fingers, the drain current contribution for each finger will be controlled by its proper extracted thermal model.

References


Chapter 4

AlGaN/GaN HEMT Small-Signal Modeling

Small-signal modeling is fundamental for large-size large-signal modeling procedure. As bottom-up modeling approach is used [1], large-signal model parameters will be in part extracted from small-signal model parameters such as nonlinear charge sources and gate currents. Therefore, the accuracy of the large-signal model nonlinear dispersive drain current is highly correlated with extracted small-signal parameters.

In this chapter, a 22-element distributed small-signal equivalent circuit model topology, as presented in Figure 4.1, is used [1]. This model is found to be suitable for the distributed physical and electrical properties in AlGaN/GaN HEMT transistors based on SiC substrates. It reflects all the linear and nonlinear effects due to distributed parasitics, trapping, and self-heating over a wide range of bias and frequency operating range. Also, it is convenient for scalability issues in large devices large-signal modeling, as it can be applied for large gate periphery devices. The small-signal model equivalent circuit topology is composed of a 12-element equivalent circuit for the extrinsic part and a 10-element equivalent circuit for the intrinsic part [2].

The extrinsic part is presented by linear extrinsic parameters. It models the device interdigitated physical layout parasitics outside the active region, which includes the RF contact pads, and the gate, drain, and source metallizations. The intrinsic part depicts the nonlinear intrinsic device active region under the gate and is presented by the intrinsic nonlinear parameters.

Two main approaches are generally used in equivalent circuit model extraction. The analytical procedure is fast [3] but may give less accuracy in the obtained model elements, whereas the optimization approach gives
more accurate model parameters [4]-[7] [1]. Also, there are other researchers working on an alternate approach; hybrid models combining both previous approaches [8]. Both ways of extraction are based on cold-FET measurement of S-parameters ($V_{DS0} = 0V$). This measurement is done while drain-source current is null, which leads to a significant reduction in the intrinsic small-signal model. Two measurement datasets of S-parameters, corresponding two gate-bias conditions, are performed to determine the extrinsic parameters. The first set is in cold pinch-off (reverse bias below pinch-off $V_{GS0} < V_p$, $V_{DS0} = 0V$) used in parasitic capacitances and inductances extraction. The second set is in cold forward (gate bias $V_{GS0} > 0V$, $V_{DS0} = 0V$) used in parasitic series resistance extraction.

![Figure 4.1](image)

**Figure 4.1** 22-element small-signal distributed equivalent circuit model for AlGaN/GaN HEMT [1].

### 4.1 Extrinsic Parameters Extraction

The extrinsic model parameter extraction procedure is the key for a successful and accurate large-signal model extraction of the HEMT device. Without a physical meaningful topology and proper extraction of these bias independent extrinsic elements, the scalability of model parameters will fail, and the extraction of accurate intrinsic model frequency independent elements is not possible [4].

The equivalent circuit of the extrinsic part (see **Figure 4.1**) is a 12-element model. Three capacitors $C_{pgi}$, $C_{pdi}$, and $C_{gdi}$ describe the effect of the inter-electrode and crossover distributed parasitic capacitance due to source air-bridge connection. Three capacitors $C_{pga}$, $C_{pda}$, and $C_{gda}$ represent
pad connections parasitics, and finally, three parasitic resistances $R_{gs}$, $R_{gd}$, and $R_{sd}$, and three inductances $L_{gs}$, $L_{sd}$ and $L_{gd}$ at the gate, source and drain contacts have also been included to model the resistive and inductive effects.

The optimization procedure, used in this work, is based on the minimization of an error function of the measured and equivalent model calculated S-parameters. It is dependent on measurement-correlated starting values, which are obtained from cold pinch-off and cold forward S-parameters measurement. These measurements are performed under an appropriate frequency range [2]. The upper frequency limit is determined for each device size to extract accurate model parameters; it decreases with device size increase. To avoid optimal local minima solutions, a robust and reliable multi-plane data fitting and bidirectional search techniques have been considered [6] [1] [9].

In the following section, the measurement-correlated starting values procedure is carried out. These values will be used in an optimization search algorithm to extract optimal model parameters. The device used for the extraction is a 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT on SiC substrate with a gate length of 0.5 µm.

### 4.1.1 Extrinsic Measurement-Correlated Starting Values

The measurement-correlated starting values estimation for final optimization procedure is described by Figure 4.2. First, the total drain, gate and source capacitances of a reduced equivalent circuit model are defined through the conversion of cold pinch-off S-parameters measurements to Y-parameters. Second, a convenient distribution of the total capacitances is investigated for each branch, meanwhile series inductances are evaluated for each distribution. Then, series resistances are evaluated and resulting extrinsic values are stored for each capacitance distribution, for which an error objective function is evaluated between simulated and measured cold pinch-off S-parameter measurements. A minimum measurement-correlated error is obtained corresponding to the measurement-correlated starting values. These, will be used in the optimization process of model parameters. In the following section, more details are given for each step.
Figure 4.2 Measurement-Correlated Extrinsic Starting Values Diagram.
4.1.2 Total Branch Capacitances Determination from Low Frequency Data

Under cold pinch-off condition ($V_{GS} < V_p$ and $V_{DS} = 0V$) the active region of the AlGaN/GaN HEMT device in the equivalent circuit model (Figure 4.1) can be reduced to the model presented in Figure 4.3. The drain current source and the output channel conductance are eliminated.

![Equivalent Circuit Model](Image)

Figure 4.3 22-element distributed model under pinch-off.

To calculate total branch capacitances, Figure 4.3 may be reduced further. At low frequency range [1], the model topology is reduced to the capacitive equivalent model presented in Figure 4.4. The inductive as well as resistive components in series with the capacitances have been neglected since their impedance will be small compared to that of the capacitance [6]. Therefore, the gate-drain, gate-source and drain-source total branch capacitances can be written respectively as

$$C_{gdo} = C_{gda} + C_{gdi} + C_{gd}$$  \hspace{1cm} (4.1)

$$C_{gso} = C_{pga} + C_{pgi} + C_{gs}$$  \hspace{1cm} (4.2)

$$C_{dso} = C_{pda} + C_{pdi} + C_{ds}$$  \hspace{1cm} (4.3)

where $C_{gd}$, $C_{gs}$ and $C_{ds}$ are the small-signal model intrinsics. Furthermore, the Y-parameters of Figure 4.4 can be expressed as
By converting cold pinch-off S-parameter measurements to Y-parameters, using (4.4), (4.5) and (4.6), the total gate-source, drain-source and gate-drain capacitances ($C_{gd0}$, $C_{gs0}$ and $C_{ds0}$) are directly estimated from the low frequency admittance matrix. This is done by plotting the imaginary parts of $Y_{11}$, $Y_{22}$ and $Y_{12}$ versus $\omega$. The total capacitances are just the slope of the linear plots.

### 4.1.3 Capacitance Distribution Determination through Iterative Scan

In this section, further assumptions and simplifications are made to extract a physically supported branch capacitances distribution. An iterative scan for each branch capacitances distribution is operated with the calculation of an error function at each scan step. Series inductances and resistances are extracted for each scan step through the stripped equivalent circuit in Figure 4.5. The convenient distribution of the capacitances is obtained through the evaluation of the objective function minimum error. Therefore, the extrinsic starting values of the optimization process for distributed capacitances and series inductances are selected to be associated to the corresponding minimum error between measured and simulated.
pinch-off S-parameters. In the following part, more details about the extraction steps is presented.

![Diagram](image)

**Figure 4.5** Cold pinch-off T-network equivalent circuit representation of 22-element model.

The total branch capacitances being identified, an iterative routine scans the outer pad capacitances ($C_{pga}$, $C_{pda}$, $C_{gda}$) while evaluating the inner capacitances using (4.1) - (4.3). The distributed capacitances extraction process can be summarized as follows [6].

- The gate pad capacitance $C_{pga}$ is assumed to be equal to the drain pad capacitance $C_{pda}$ ($C_{pga} = C_{pda}$), and scanned from 0 to $C_{Max} = 0.5 \cdot C_{ds0}$. This is typically true for on-wafer and in-fixture devices, whereas an upper bound for $C_{max}$ should be defined in connection with the extracted inductances change of sign [6].
- The gate-drain inter-electrode capacitance $C_{gdi}$ is assumed to be twice of pad capacitance $C_{gda}$ value ($C_{gdi} = 2C_{gda}$), where $C_{gda}$ is scanned from 0 to ($0.5 \cdot C_{gd0}$).
- The gate-source and the gate-drain depletion region capacitances are assumed to be equal under pinch-off ($C_{gs} = C_{gd}$) assuming symmetrical AlGaN/GaN devices.
- $C_{pdi}$ is significantly large in AlGaN/GaN HEMTs. therefore, one more approximation that is found to be consistent is ($C_{pdi} = 3C_{pda}$) [1].
Using these assumptions, all capacitances can be obtained with (4.1) - (4.3) at each iteration step. For medium and high frequency range, the equivalent circuit of the proposed model at cold pinch-off is shown in Figure 4.5. The outer pad capacitances, \( C_{pga} \) and \( C_{pda} \) are deembedded from the measured Y-parameters than converted to Z-parameters. The remaining gate, drain and source branch capacitances are represented by \( C_g \), \( C_d \), and \( C_s \), respectively, in the stripped Z-network, from which the inductances, \( L_g \), \( L_d \) and \( L_s \) are estimated as will be presented in the next section. The \( \delta Z_g \), \( \delta Z_d \), and \( \delta Z_s \) terms represent correction terms related to the intrinsic parameters of the model.

### 4.1.4 Inductances Values Extraction in the Iterative Scan

The parasitic series inductances can be estimated from the stripped Z-parameters at higher frequencies (>3 GHz). The resulting impedance equations of the Z-parameters equivalent network, presented in Figure 4.6, are described by

\[
Z_{zz} = R + j\omega(L + L_s) + \frac{1}{j\omega(C + C_s)} + \delta Z
\]

(4.7)

\[
Z_{zd} = R + j\omega(L + L_s) + \frac{1}{j\omega(C + C_s)} + \delta Z
\]

(4.8)

\[
Z_{dz} = Z_{zd} = R + j\omega L_s + \frac{1}{j\omega C_s} + \delta Z
\]

(4.9)

where

\[
\delta Z = \delta R + \delta R_s + j\omega(\delta L + \delta L_s)
\]

(4.10)

\[
\delta Z = \delta R_d + \delta R_s + j\omega(\delta L_d + \delta L_s)
\]

(4.11)

\[
\delta Z = \delta R_s + j\omega L_s
\]

(4.12)
By discarding the correction terms as presented in Figure 4.7, multiplying (4.7) - (4.9) by $\omega$ and taking the imaginary parts, gives

\[
\text{Im}[\omega Z_{11}] = (L_g + L_s)\omega^2 - \left( \frac{1}{C_g} + \frac{1}{C_s} \right)
\]  
(4.13)

\[
\text{Im}[\omega Z_{22}] = (L_d + L_s)\omega^2 - \left( \frac{1}{C_d} + \frac{1}{C_s} \right)
\]  
(4.14)

\[
\text{Im}[\omega Z_{12}] = L_s\omega^2 - \frac{1}{C_s}
\]  
(4.15)
By plotting $\text{Im}[\omega \cdot Z_{ij}]$ versus $\omega^2$, estimated values of the extrinsic inductances values ($L_g$, $L_d$, $L_s$) are extracted from the slope of the equivalent linear curve fitting traces as shown in Figure 4.8. These inductances are extracted for each pad capacitance distribution. The resulting values are stored in a vector.

![Figure 4.8](image)

**Figure 4.8** Cold pinch-off inductance estimation from Z-network equivalent circuit for 0.5 µm AlGaN/GaN HEMT with 3.2-mm (8 x 400 µm) gate width.

### 4.1.5 Extrinsic Resistances Estimation in the Iterative Scan

After deembedding pad capacitances ($C_{pga}$, $C_{pda}$, and $C_{gda}$) and series inductances ($L_g$, $L_d$, $L_s$), as described in previous section, the interelectrode capacitances are deembedded using the equivalent Y-network model presented in Figure 4.9. The series resistances are obtained from the real part of the resulting Z-parameters as described in (4.7), (4.8), and (4.9) after conversion. It is reported in [6] and supported by [1] that the incomplete deembedding of the extrinsic reactances introduces nonlinear frequency dependence in the real part of resulting Z-parameters. Moreover, to reduce this effect, the deembedded real part of (4.7) - (4.9) are multiplied by $\omega^2$. This gives
\[ \omega^2 \text{Re}[Z_{11}] = \omega^2 (R_g + R_s) \]  
(4.16)

\[ \omega^2 \text{Re}[Z_{22}] = \omega^2 (R_d + R_s) \]  
(4.17)

\[ \omega^2 \text{Re}[Z_{12}] = \omega^2 R_s \]  
(4.18)

Figure 4.9 The equivalent pinch-off stripped Y-parameter network used for deembedding inter-electrode capacitances after deembedding series inductances.

In Figure 4.10, the estimated values of \( R_s \), \( R_d \) and \( R_g \) are extracted through the evaluation of the slope of curves \( \omega^2 \text{Re}[Z_{12}] \), \( \omega^2 \text{Re}[Z_{22}] \) and \( \omega^2 \text{Re}[Z_{11}] \) versus \( \omega^2 \), respectively, as described by (4.16) - (4.18).
4.1.6 Minimum Error Determination and Reactive Elements Estimation

After all the elements of the equivalent circuit of the cold pinch-off small signal model have been estimated, a residual fitting error function is evaluated using measured and corresponding simulated S-parameters. Therefore, for each step in the iterative capacitances scan process a residual error ($\varepsilon$) is calculated, as presented in Figure 4.11. Hence, the best initial starting values for the extrinsic capacitances and inductances, which correspond to $C_{pga}$ and $C_{gda}$ distribution with the lowest residual error ($\varepsilon_{min}$) are selected.
4.1.7 Extrinsic Resistances Starting Value

To extract series branches resistances starting values (R\textsubscript{g}, R\textsubscript{d}, and R\textsubscript{s}), cold forward S-parameter measurements at relatively high gate voltage (V_{GS0} > 2.0V) are used. The forward voltage is relatively high as compared to AlGaAs/GaAs technology to cancel the influence of the intrinsic gate built-in Schottky contact capacitance [6].

Similar to series resistances extraction in Section 4.1.5, after de-embedding the starting values of the extrinsic capacitances and inductances corresponding to minimum error from the cold forward measurements, the starting values of series resistances R\textsubscript{g}, R\textsubscript{d} and R\textsubscript{s} are obtained from the resulting Z-parameter network presented in Figure 4.9 using (4.16) - (4.18).
The resistances starting values extracted from the curves slope are shown in Figure 4.12 for 3.2-mm AlGaN/GaN HEMT.

![Figure 4.12](image_url)

**Figure 4.12** Cold forward measurements based series extrinsic resistances starting values estimation through slope evaluation of presented curves of a 8 x 400-µm gate width AlGaN/GaN HEMT and 0.5-µm gate-length on SiC.

<table>
<thead>
<tr>
<th>Extrinsic Parameters</th>
<th>Intrinsic Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{pga} = 114.4$ fF</td>
<td>$L_i = 90.706$ pH</td>
</tr>
<tr>
<td>$C_{pda} = 114.4$ fF</td>
<td>$L_d = 172.75$ pH</td>
</tr>
<tr>
<td>$C_{gda} = 17.631$ fF</td>
<td>$L_s = 2.6684$ pH</td>
</tr>
<tr>
<td>$C_{pdi} = 457.58$ fF</td>
<td>$R_g = 2.3408$ Ω</td>
</tr>
<tr>
<td>$C_{pgi} = 518.7$ fF</td>
<td>$R_d = 2.6025$ Ω</td>
</tr>
<tr>
<td>$C_{gdi} = 35.262$ fF</td>
<td>$R_s = 0.42852$ Ω</td>
</tr>
<tr>
<td>$C_{gs} = 670.29$ fF</td>
<td>$G_m = 0.0$ mS</td>
</tr>
<tr>
<td>$C_{ds} = 0.0$ fF</td>
<td>$G_{ds} = 0.0$ mS</td>
</tr>
<tr>
<td>$C_{gd} = 1.6414$ pF</td>
<td>$G_{gds} = 0.0$ mS</td>
</tr>
<tr>
<td>$R_i = 7.8989$ Ω</td>
<td>$R_{sd} = 0.25773$ Ω</td>
</tr>
<tr>
<td>$R_g = 0.25773$ Ω</td>
<td>$\tau = 0.0$ ps</td>
</tr>
</tbody>
</table>

**Table 4.1** Starting parameter values of a 3.2-mm AlGaN/GaN HEMT with an 8 x 400 µm gate-width derived from measurement (pinch-off and forward).

At this point, all extrinsic elements starting values are estimated for the small-signal model. These are input to the optimization routine to get the optimized final small signal model parameters. The starting parameter values for 22-element model using cold pinch-off and cold-forward S-parameter measurements are given in Table 4.1.
4.2 Verification of Extrinsic Starting Values

Using the measurement-correlated extraction algorithm in the extraction of the starting values for final optimization procedure will reduce largely the risk of being trapped in a local minimum, as described in the next section. This is confirmed by the good agreement of the simulated versus measured S-parameters as shown in Figure 4.13 and Figure 4.14 for cold pinch-off and cold forward, respectively, except a small discrepancy in \((S_{22})\) at higher frequency range. This proves the high quality of these starting values.

*Figure 4.13* Cold pinch-off S-parameter verification. Comparison between S-parameter measurements (markers) and simulated S-parameters (lines) using estimated starting values of small-signal model of a 3.2-mm GaN HEMT with \(V_{GSO} = -4.5\) V.
Figure 4.14 Cold forward S-parameter verification. Markers denote measured S-parameters, lines denote simulated S-parameters using estimated starting values of small-signal model.

4.3 Extrinsic Model Parameters Optimization

After the definition of the starting values of the model parameters, the new optimization technique developed in our department, proposed in [10] [5] [11] and enhanced in [6] and [1], is used.

The model parameter optimization strategy is based on bidirectional optimization technique to reduce dimension of the searching space in such a way that only the extrinsic parameters are varied (optimized) in the optimizing process; with the assumption that generated extrinsic starting value are in the vicinity of the optimized values.

The optimization process starts by assigning iteratively values for the extrinsic parameters. These are deembedded from measured S-parameters and converted to Y-parameters to extract the equivalent intrinsic parameters. As mentioned previously in Section 4.1.1, using multi-plane data fitting, the intrinsic model parameters are evaluated for each iteration.
step. The resulting small signal model is simulated and results used to evaluate an objective function associated with measured S-parameters.

As the optimization process is multidimensional, to avoid local minima trapping, a careful formulation for the objective function is essential. Therefore, the magnitude of the error between the measured and simulated S-parameters is expressed as [6]

$$\varepsilon_{ij} = \left| \frac{\text{Re}(\delta S_{ij,n}) + \text{Im}(\delta S_{ij,n})}{W_{ij}} \right|, \quad i,j = 1,2; \quad n = 1,2,\ldots,N$$

(4.19)

where

$$W_{ij} = \max |S_{ij}|, \quad i,j = 1,2; \quad i \neq j$$

(4.20)

$$W_{ii} = 1 + |S_{ii}|, \quad i = 1,2$$

(4.21)

$\delta S$ is the difference between measured and simulated S-parameter. $N$ is total number of data points. $W_{ij}$ is a reflection coefficient weighting factor, it reflects higher measurement uncertainty regions. Therefore, the scalar S-parameters fitting error is defined as [1]

$$\varepsilon_s = \frac{1}{N} \sum_{n=1}^{N} \left\| \varepsilon(f_n) \right\|$$

(4.22)

where

$$\varepsilon(f_n) = \begin{bmatrix} \varepsilon_{11}(f_n) & \varepsilon_{12}(f_n) \\ \varepsilon_{21}(f_n) & \varepsilon_{22}(f_n) \end{bmatrix}$$

(4.23)

and $f_n$ is frequency point of operation.

According to [10] and [1], this S-parameter based fitting error objective function may result to unphysical solution. Therefore, other performance criteria are added. For AlGaN/GaN power amplifiers application, the output and input impedance, the device gain, and stability factor are included in the optimization as a function of S-parameters. The application related new fitting error objective function is expressed as [1]

$$\varepsilon = \sqrt{\frac{1}{3} \left( \varepsilon_s^2 + \varepsilon_K^2 + \varepsilon_G^2 \right)}$$

(4.24)
where

\[
\varepsilon_K = \frac{1}{N} \sum_{k=1}^{N} |K_{meas} - K_{sim}|
\]

(4.25)

\[
\varepsilon_G = \frac{1}{N} \sum_{m=1}^{N} |G_{meas} - G_{sim}|
\]

(4.26)

with \(\varepsilon_G\) the gain fitting error, where \(G_{meas}\) and \(G_{sim}\) are measured and simulated S-parameter gains, respectively. \(\varepsilon_K\) is the output stability factor fitting error, where \(K_{meas}\) and \(K_{sim}\) are measured and simulated S-parameter stability factors, respectively.

The objective function in (4.24) is minimized using a modified Simplex optimization algorithm [10]. The optimized parameter values for 22-element model using cold pinch-off (for the extraction of the parasitic reactances) and cold-forward (for the extraction of the parasitic resistances) S-parameter measurements are given in Table 4.2.

**Table 4.2** Optimized parameter values of a 3.2-mm (8 x 400 \(\mu\)m) GaN HEMT

<table>
<thead>
<tr>
<th>Extrinsic Parameters</th>
<th>Intrinsic Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{pga}) = 162.88 fF</td>
<td>(C_{gs} = 590.53) fF (G_m = 0.0) mS</td>
</tr>
<tr>
<td>(C_{pda}) = 130.12 fF</td>
<td>(C_{ds} = 1.0051) fF (G_{ds} = 0.0) (\mu)S</td>
</tr>
<tr>
<td>(C_{gda}) = 53.643 fF</td>
<td>(C_{gd} = 1414.3) fF (G_{gd} = 0.0) mS</td>
</tr>
<tr>
<td>(C_{pgi}) = 549.14 fF</td>
<td>(R_i = 3.8265) (\Omega) (R_{gd} = 0.0) (\Omega)</td>
</tr>
<tr>
<td>(C_{pdi}) = 430.14 fF</td>
<td>(R_d = 0.95458) (\Omega) (\tau = 0.0) ps</td>
</tr>
<tr>
<td>(C_{gdi}) = 225.73 fF</td>
<td>(R_s = 0.63374) (\Omega)</td>
</tr>
</tbody>
</table>

- It is clear that extracted source inductance \(L_s\) is very small as compared to gate and drain inductances \(L_g\) and \(L_d\), which is physically true.
- Also the extracted source series resistance inductance \(R_s\) is small as compared to gate and drain series resistances \(R_g\) and \(R_d\), which is also physically expected.
- No negative optimized small-signal model parameters have been delivered by the algorithm; this reflects the sufficient measurement frequency range that has been selected.
- It can be observed that the optimized values are close to the starting values; this confirms the consistency of the approach of using cold pinch-off and cold forward S-parameter measurement to obtain
reactive and resistive starting values for the parasitic extrinsic elements, respectively.

- The accuracy of the extrinsic parameters optimization procedure is shown in Figure 4.15 through the comparison of simulated and measured S-parameters taken below pinch-off, at which extrinsic capacitances and inductances are extracted.

![Figure 4.15](image.png)

**Figure 4.15** Pinch-off S-parameter fitting with optimized element values equivalent circuit model for a 3.2-mm AlGaN/GaN HEMT with an 8 x 400 μm gate-width. Markers denote measured S-parameters, lines denote simulated S-parameters using optimized parameters.

At this point, all extrinsic elements are estimated and can be de-embedded from the measured S-parameter. This leads to the intrinsic transistor Y-parameters, and, thus, the intrinsic elements of the model can be determined.
4.4 Bias-Dependent Intrinsic Parameters Extraction

Now that all the optimized extrinsic small-signal model parameters are available, frequency independent bias dependent intrinsic parameters are calculated from resulting deembedded Y-parameters equivalent circuit presented in Figure 4.1. These parameters can be extracted from either closed form analytical equations or a linear data fitting. To get frequency independent intrinsic parameters mainly for ohmic region bias conditions, these elements are evaluated using linear data fitting with a special formulation of the intrinsic Y-parameters. The extraction procedure is detailed in [2] [6] [1], a resume of this procedure and obtained results will be given in the following subsections.

4.4.1 Gate-Source Branch Elements Extraction

The intrinsic parameters can be determined from the intrinsic Y-parameters as will be described below through linear data fitting techniques following the procedure in [1].

- **Extraction of $C_{gs}$**

The $Y_{gs}$ admittance of the intrinsic gate-source branch can be written as

$$Y_{gs} = Y_{i,11} + Y_{i,12} = \frac{G_{gsf} + j\omega C_{gs}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}}$$

(4.27)

By defining the operator $D_{gs}$ as

$$D_{gs} = \frac{|Y_{gs}|^2}{\text{Im}[Y_{gs}]} = \frac{G_{gsf}^2}{\omega C_{gs}} + \omega C_{gs}$$

(4.28)

$C_{gs}$ can be obtained from the slope of the curve for $(\omega \cdot D_{gs})$ versus $\omega^2$ by linear fitting, where $\omega$ is the angular frequency.

- **Extraction of $R_i$**

By defining the operator $D_{i}$ as

$$D_{i} = \frac{Y_{gs}}{\text{Im}[Y_{gs}]} = \frac{G_{gsf}(1 + R_i G_{gsf})}{\omega C_{gs}} + \omega R_i C_{gs} - j$$

(4.29)
\( R_i \) can be determined from the plot of the real part of \( \omega D_i \) versus \( \omega^2 \) by linear fitting.

- **Extraction of \( G_{gsf} \)**

\( G_{gsf} \) can be determined from the real part of \( Y_{gs} \) in (4.27) at low frequency range (MHz).

### 4.4.2 Gate-Drain Branch Element Extraction

Similarly, following the same procedure applied to gate-source branch, the admittance for the intrinsic gate-drain branch \( Y_{gd} \) can be written as

\[
Y_{gd} = -Y_{i2} = \frac{G_{gdf} + j\omega C_{gd}}{1 + R_{gd} G_{gdf} + j\omega R_{gd} C_{gd}}
\]  

**Extraction of \( C_{gd} \)**

To extract \( C_{gd} \), first we define the operator \( D_{gd} \) as

\[
D_{gd} = \frac{|Y_{gd}|^2}{\text{Im}[Y_{gd}]} = \frac{G_{gdf}^2}{\omega C_{gd} + \omega C_{gd}}
\]  

\( C_{gd} \) can be determined from the slope of the curve for \( \omega D_{gd} \) versus \( \omega^2 \) by linear fitting.

- **Extraction of \( R_{gd} \)**

Also by changing the operator expression to \( D'_{gd} \) as

\[
D'_{gd} = \frac{Y_{gd}}{\text{Im}[Y_{gd}]} = \frac{G_{gdf} (1 + R_{gd} G_{gdf})}{\omega C_{gd}} + \omega R_{gd} C_{gd} - j
\]  

\( R_{gd} \) can be determined from the plot of the real part of \( (\omega \cdot D'_{gd}) \) versus \( \omega^2 \) by linear fitting.

- **Extraction of \( G_{gdf} \)**

\( G_{gdf} \) is determined directly from the real part of \( Y_{gd} \) in (4.32) at the low frequency range (MHz).
4.4.3 Drain-Source Branch Elements Extraction

Following the development above, the admittance of the intrinsic transconductance branch $Y_{gm}$ can be expressed as

$$Y_{gm} = Y_{i,21} - Y_{i,12} = \frac{G_m e^{-j\omega \tau}}{1 + R_f G_{gs} f + j\omega C_{gs}}$$  \hspace{1cm} (4.33)

- **Extraction of $G_m$**

To extract the transconductance $G_m$, a similar operator $D_{gm}$ is defined as

$$D_{gm} = \frac{Y_{gs}}{Y_{gm}} = \left(\frac{G_{gs}}{G_m}\right)^2 + \left(\frac{C_{gs}}{G_m}\right)^2 \omega^2$$  \hspace{1cm} (4.34)

$G_m$ is estimated from the slope of the curve of the operator $D_{gm}$ versus $\omega^2$ by linear fitting.

- **Extraction of $\tau$**

For the transit time delay $\tau$, a related operator expression is defined,

$$D_{\tau} = (G_{gs} f + j\omega C_{gs}) \frac{Y_{gm}}{Y_{gs}} = G_m e^{-j\omega \tau}$$  \hspace{1cm} (4.35)

$\tau$ is evaluated from the slope of the plot of the phase of operator $D_{\tau}$ versus angular frequency $\omega$ by linear fitting.

- **Extraction of $C_{ds}$**

The drain-source capacitance $C_{ds}$ can be evaluated from the admittance of the intrinsic drain-source branch $Y_{ds}$ given by

$$Y_{ds} = Y_{i,22} + Y_{i,12} = G_{ds} + j\omega C_{ds}$$  \hspace{1cm} (4.36)

The drain-source capacitance $C_{ds}$ is evaluated from the plot slope of the drain-source admittance imaginary part $\text{Im}[Y_{ds}]$ versus angular frequency $\omega$ by linear fitting.

- **Extraction of $G_{ds}$**

Due to the frequency-dependent effect in the output conductance, $G_{ds}$ is determined from the curve of $(\omega \cdot \text{Re}[Y_{ds}])$ versus $\omega$ by linear fitting.
The extracted bias dependent intrinsic elements as function of extrinsic drain and gate voltages are shown in Figure 4.16 and Figure 4.17. The plots show that the extracted intrinsic parameters are physically consistent and smooth.

As shown in Figure 4.16, the drain gate capacitance $C_{gd}$ reflects the extension of the depletion region into the gate-drain space. While increasing $V_{DS}$, the drain voltage $C_{gd}$ decreases due to an increase in the depletion region. The gate source capacitance $C_{gs}$ increases as $V_{GS}$ increases; it reflects the gate-metallization to the 2DEG HEMT channel charge capacitance. Furthermore, $C_{gs}$ increases as the drain voltage $V_{DS}$ increases due to related lateral electric field which accelerates charge carriers in the channel to scatter into the barrier layer [12].

The drain source capacitance $C_{ds}$ is relevant in the linear region due to high-field reduction. It reflects depletion layer high-field part which separates the source and drain electrodes. The problem of negative $C_{ds}$ capacitances, encountered in the ohmic region (at low $V_{DS}$) using other developed small-signal model extraction procedures as in [4] and [13], appears to be solved using this approach and reflects the reliability of this small-signal extraction procedure.

The transconductance $G_m$ is related to both channel charge density and electron velocity. It increases as the gate voltage $V_{GS}$ increases, and also increases with increasing drain voltage $V_{DS}$ in the linear region ($V_{DS} < V_{DS,sat}$). As the electric field strength reaches saturation in 2DEG HEMT channel ($V_{DS} > V_{DS,sat}$), $G_m$ saturates due to electron velocity saturation [14].

The remaining extracted bias dependent parameters $R_i$, $R_{gd}$, $G_{ds}$, and $\tau$ are presented in Figure 4.17. The channel resistance $R_i$, also called charging resistance, models the resistance of the channel at low field region under charged gate source capacitance $C_{gs}$ [14]. The charging resistance $R_{gd}$ models the symmetrical distribution of the depletion region under the gate in the ohmic-forward region. It is expected to have a similar behavior as $R_i$ in this region.

The output conductance $G_{ds}$ depicts the variation of the drain current with the drain voltage. Therefore, at drain current nearly constant (saturation region) $G_{ds}$ is shown to be very small.
Figure 4.16 Extracted bias-dependent capacitances ($C_{gs}$, $C_{gd}$, $C_{ds}$) and transconductance ($G_m$) as a function of the extrinsic voltages for 3.2-mm AlGaN/GaN HEMT.

Figure 4.17 Extracted $R_i$, $R_{gd}$, $G_{ds}$, and $\tau$ as a function of the extrinsic voltages for 3.2-mm AlGaN/GaN HEMT.
The transit time $\tau$ is a measure of the channel electron transit time under the depletion region [14]. By increasing the drain-gate voltage, the transit time $\tau$ increases due to the extension of the depletion region in the gate-drain area. Therefore, $\tau$ increases with either by increasing the drain voltage or decreasing the gate voltage, as shown in Figure 4.17.

Furthermore, all data surfaces of the extracted elements are extrapolated to higher range of $V_{GS}$ and $V_{DS}$ outside the measured data range, to include higher power dissipation region outside the normal operating region of the device.

References


Chapter 5

AlGaN/GaN HEMT Electrothermal Large-Signal Characterization

Large-signal electrothermal characterization is essential in modeling high power AlGaN/GaN HEMT devices for power amplifiers applications in modern wireless communication basestations. The main success points in characterization process reside in the derivation of the nonlinearities for model implementation of the HEMT. These are mainly the nonlinear charges and the nonlinear dispersive drain current in the large-signal equivalent circuit model implementation.

There are distinct characterization techniques, based on the model parameter to be extracted in modeling large-signal HEMT devices for power amplifiers applications. Standard CW S-parameter measurements are used for parasitic elements in small-signal equivalent model parameter extraction and charge sources in the nonlinear large-signal model. Whereas, pulsed I(V) measurements are used for large-signal nonlinear drain current fitting functions, and finally pulsed I(V) transient measurements for drain, gate, and thermal time constants extraction for transient large-signal equivalent circuit model. These techniques provide improved large-signal simulation accuracy; the model nonlinearities are constructed from pulsed measurements that best predict the device RF response under real highly linear and efficient RF power amplifier applications.

In the following sections a deep investigation of the pulsed I(V) measurements and pulsed transient measurements is carried out for large-signal modeling of AlGaN/GaN HEMT devices. These characterizations are required for developing a dispersive and accurate large-signal model in power amplifier applications. First, an overview of the pulsed I(V) characterization fundamentals, system setup, and database requirements for
large-signal model development are presented. Then, pulsed I(V) dispersion effects characterization is handled for RF (dynamic) nonlinear drain current model implementation. Surface trapping, buffer trapping, and self-heating effects are separately determined as function of quiescent bias point voltages under fixed and variable temperature. Next, the pulsed transient characterization is performed to extract time constants for transient surface trapping, buffer trapping and self-heating under low frequency excitations.

Finally, the last part is dedicated to thermal resistance characterization based on pulsed I(V) measurements and static DC under variable channel chuck temperature controller, from which higher-order thermal model is proposed for the large-signal model implementation.

5.1 Pulsed I(V) Characterization Fundamentals

For characterizing large-signal model for large AlGaN/GaN device sizes, with significant self-heating and trapping effects, several types of device characterizations are required. Its efficiency depends on the resulting drain current nonlinear dispersion implemented model accuracy. In characterizing high power AlGaN/GaN HEMT devices drain current nonlinearities, pulsed I(V) measurement is the most relevant regarding conventional CW S-parameter measurements [1] [2]. It permits a detailed in-depth characterization of the drain current nonlinearities; trapping and self-heating effects can be isolated and implemented separately.

Pulsed DC characterization technique enables us also to perform measurements at higher power levels compared to CW technique. This makes it suitable for characterizing devices at higher rating drain current operating points. Moreover, pulsed transient measurements are required to obtain time constants of the large-signal equivalent circuit model for drain, gate and thermal transient effects. Breakdown characteristics of power devices can be obtained too using this type of characterization.

5.1.1 Pulsed Measurements Principle

Pulsed I(V) measurement is performed to obtain the current conduction characteristics of the HEMT device unaltered by any reactive current related to charge variations. It is done starting from a well defined quiescent bias point \((V_{GS0}, V_{DS0})\), depending on the targeted device
application. Pulsed I(V) measurements are made at a pulsed-to points \( (V_{GS}, V_{DS}) \) different from the bias condition, as shown in Figure 5.1 [3]. The pulsed drain measurements are represented by traces depending on the pulsed-to points polarization and magnitude \( (V_{GS}, V_{DS}) \) with respect to the quiescent bias point \( (V_{GS0}, V_{DS0}) \).

![Figure 5.1 Pulsed I(V) fundamentals used for AlGaN/GaN HEMT characterization [3]. Pulsed I(V) characterization for this quiescent bias point \( (V_{GS0}, V_{DS0}) \) obtained through scan for pulsed-to gate and drain voltages \( (V_{GS}, V_{DS}) \).](image)

The device temperature and trapping effects are determined by the quiescent bias condition. The current is measured after the fast processes have adapted to the new operating condition, but before the slow processes happened. As shown in Figure 5.2 [3], the typical time response intervals to an ideal voltage step response. Phase (I) is related to fast processes and reactive currents adaptation; typically in semiconductors it is in the range of picoseconds. Phase (II) is the pulsed I(V) measurement time interval of the pulsed-to dynamic point. It is the transition time after the fast processes are adjusted and slow processes still belongs to the quiescent bias condition. In phase (III) is the pulsed transient measurement time interval of the pulsed-to quiescent bias point. The slow processes (i.e. surface and buffer charge trapping and self-heating effect) are adjusting to the new pulsed-to quiescent bias point. Phase (IV) corresponds to the steady-state (DC) of the new pulsed-to point. It is measured after the adjustment of transient slow processes.

Accordingly, phase (II) is used in dynamic pulsed I(V) measurements. The pulse rate used should be fast enough to exclude dispersion effects and slow enough to exclude reactive currents. Therefore, the pulsed I(V) drain current is measured from a pulsed-to dynamic operating conditions. It is
dependent upon the pulsed from quiescent bias point and reflects the device operation under its intended application (i.e. PA, mixer, RF switch, limiter) [3] [4].

![Figure 5.2](image)

**Figure 5.2** Typical FET drain current response in a pulsed measurement system (after [3]). The current in region III may decrease or increase depending on the dispersion effect present at selected quiescent bias and pulsed-to points.

### 5.1.2 Pulsed System Set-Up Requirements

In characterizing power AlGaN/GaN HEMTs, measurement system with two pulse generating instruments is required. The drain and gate of the device are subjected to synchronized voltage pulses from reference quiescent bias voltages. The resulting current response at the drain and gate ports of the HEMT device is then sampled at the end of the pulse. It is worth to mention here that characterization systems based on single pulse instrument system are not suited for FET devices. This last fixes the drain voltage to a preset DC value; it is not possible to pulse drain voltage from any DC quiescent bias point to any pulsed-to bias point [3] [5].

For AlGaN/GaN HEMTs under consideration, higher drain pulse voltages are required as these power devices can be operated at least at voltages up to 90 Volts for 3.2-mm gate width devices. These power devices also reach a drain current, $I_{DS,max}$, of about 1 A/mm. Therefore the current range of the pulse instrument must be of several amperes. In our case, the rating of the 3.2-mm is higher than the set-up measurement system limit (2A limit in Diva D265EP). This reduces the measurement data base range and introduces errors in the linear region at high current ratings or at compression point in RF output power model simulations.
Another important system requirement is to generate pulses with both negative and positive pulse amplitude polarities, and well shaped sub-microsecond range pulse widths. For each specific measurement, limits are set to the minimum pulse width for reliable measurements. Generally, narrow pulses are the most difficult to meet in pulsed measurement systems. Measurement environment should be considered in defining minimum pulse widths, such as delays added to applied pulse due to cables for on-wafer devices characterization. Shortest possible cable lengths are generally used to avoid invalid measurements. For the Diva D265EP measurement system, used in this work, the minimum well shaped pulse duration is 0.1 µs. Generally, it can deliver pulse durations at fixed time widths (µs) (0.1, 0.2, 0.5, 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000).

Using Diva D265EP system, the computer control software is properly designed to control the sequence of the applied gate and drain pulses. Moreover, the current and power dissipation limits are properly sensed and set within its environment. If device under test (DUT) is unstable, low inductance resistor in series with the gate, or in parallel with the drain port may be used to eliminate oscillations. The resulting measurements are automatically compensated. Sweep rate at which the drain voltage is increased per second in static DC measurements should be handled with care (slower sweep rate) in regards to thermal dissipation (to avoid thermal memory effect).

5.1.3 Pulsed System External Temperature Controller

High power dissipation is one of the main figures of merit of AlGaN/GaN HEMT technology on SiC. To characterize DUTs thermal dispersive behavior under different case temperatures and/or high dissipation quiescent bias points, an external chuck temperature controller is used. For AlGaN/GaN HEMTs large devices, RF power densities greater than 10 W/mm are reached at 2.14 GHz as compared to about 0.7 W/mm for Si-LDMOS and GaAs FETs [6]. Therefore, to accurately determine the effect of excessive RF power dissipation at arbitrary quiescent bias points, which generates high self-heating, the HEMT channel temperature should be accurately characterized, as will be discussed in the next sections.

The temperature controlled measurements will be reflected in the large-signal model implementation through the drain current fitting thermal function and the thermal model equivalent circuit. First, the pulsed I(V)
drain current from quiescent bias point \((V_{GS0}, V_{DS0}) = (0V, 0V)\) as function of case temperature are measured to isolate and characterize self-heating effect. Then, the thermal resistance are extracted from temperature controlled pulsed I(V) measurements and/or static measurements. Finally, the measurement thermal time constant is obtained from transient pulsed measurements.

The pulsed DC measurement setup used in this work uses a CASCADE probe station (Model 42), which is equipped with a chuck temperature controller that allows varying case temperature from -50°C up to 200°C.

### 5.2 Drain Current and Pulsed I(V) Characterization Fundamentals for Power Amplifiers

As described previously, dispersion refers to the fact that the dynamic (i.e. RF) behavior of HEMTs is different from their static (or DC) behavior as measured by standard test instrumentation. Dispersion is primarily originating in semiconductor material quality and the quality of device fabrication technology which affects the surface condition of the semiconductor after device or circuit fabrication [3]. It is mainly related to charge exchange with surface traps, buffer traps, and self-heating in semiconductor devices. These three dispersive mechanisms have characteristic time constants which are typically in the range of \((1 \mu s \text{ to } 1 \text{ ms})\) [3], and in the range of \((10 \mu s \text{ and } 100 \mu s)\) for trapping and \((1 \text{ ms})\) range for self-heating as reported in [7] [8].

As will be demonstrated in the next sections, the drain current is dependent on quiescent bias point voltages \((V_{GS0}, V_{DS0})\), the instantaneous (or pulsed-to) voltages \((v_{GS}, v_{DS})\), and self-heating equivalent temperature reflected in channel temperature \(T_{ch}\). In general, it can be written as

\[
i_{DS} = f(V_{GS0}, V_{DS0}, v_{GS}, v_{DS}, T_{ch})
\]

Criteria and benchmarks have to be set for pulsed system measurements in order to obtain drain current for large-signal modeling. Pulsed from quiescent bias points \((V_{GS0}, V_{DS0})\) and pulsed-to points \((v_{GS}, v_{DS})\) should be determined for each dispersive effect characterization of the drain current in microwave power amplifiers applications.
In microwaves power amplifiers, RF loadline swing is shown to match exactly the pulsed I(V) measurements characteristics. This is due to increasing knee voltage and current collapse as the quiescent bias drain and gate voltages are increased. Also, RF loadline shifts in the direction of the drain bias voltage change. This behavior cannot be characterized by multi-bias CW S-parameter measurements for large-signal devices. This type of measurements gives the small-signal properties, whereas the response of the HEMT transistor varies with the bias point voltages and temperature. The RF characterization using standard S-parameters produces incorrect drain current model in large-size AlGaN/GaN HEMT devices. Therefore, to generate the same RF loadline, pulsed I(V) and/or pulsed S-parameters measurement from the same bias point as in the RF measurement environment is used [2] [5].

Similarly, it is shown that conductances, transconductance, and higher order derivatives of the drain currents should be characterized using pulsed I(V) measurements to be correctly estimated. These parameters are essential for accurate prediction of the fundamentals, intermodulations, and harmonics output power, gain and gain compression [3] [5] [9].

In order to implement these HEMT device characteristics in CAD environment, drain current dispersion mechanisms should be characterized using this equivalent pulsed I(V) measurements technique. Therefore, to use pulsed I(V) characterization in implementing accurate drain current model, surface trapping, buffer trapping, and self-heating effects should be characterized under the quiescent bias point (V_{GS0},V_{DS0}).

Therefore, due to unique response of the pulsed I(V) measurement to quiescent bias point conditions, a particular set of bias points are of interest in modeling drain current for targeted large-signal power amplifier applications. These set of bias points should include all dispersion effects in the nonlinear drain current formulation. As self-heating is significant only in active bias regions (non-zero drain current), pulsed I(V) measurements from quiescent bias point (V_{GS0} = 0V, V_{DS0} = 0V) have negligible trapping effects. The electric field is negligible and the traps are not occupied. This quiescent bias point, considered as a reference, delivers the maximum drain current in RF power amplifiers applications. To characterize the dispersive effects in the nonlinear drain current, the quiescent bias point voltages are changed accordingly to obtain separate dispersive bias-dependent fitting function [10].
In the next sections, the characterization of the large-signal drain current model will be illustrated. The pulsed I(V) measurements are used to determine the separate bias-dependent dispersive fitting functions for large-signal drain current modeling. This will be implemented in the next chapter in the nonlinear drain current expression.

5.3 Pulsed I(V) Trapping and Self-Heating Dispersive Effects Characterization

From previous sections, it is shown that to model accurately the high power AlGaN/GaN HEMT large-signal drain current as a function of the dispersive effects, pulsed I(V) measurements at appropriate quiescent bias points and distinct channel temperatures have to performed. Moreover, the drain current is dependent on both instantaneous (RF) and average (quiescent bias) drain and gate voltages. These lead us to investigate the set of measurements that best describes the drain current variations with the isolated sources of dispersive effects.

Therefore, appropriate independent pulsed I(V) measurements have to be defined to characterize the isolated dispersive effects. The drain current is assumed, under these independent measurements, to be affected by only one dispersion effect (surface trapping, buffer trapping, or self-heating).

To separately characterize trapping effects, the thermal effects should be excluded. This is achieved through dynamic pulsed I(V) measurements at bias points with constant temperature [11]. The differences obtained in resulting pulsed dynamic IV curves are attributed to only charge trapping effects. Therefore, measurements should be done at different bias points with either negligible power dissipation or lie on the same dissipated power hyperbola. The first set of bias points can be operated in the pinch-off region, whereas, the second set can be obtained along any active region constant power dissipation curve. The drain trapping and gate trapping effects are separately characterized using appropriate bias points as will be described in the next section [12].

The derivation of the fitting parameters of the dispersive nonlinear drain current expression, presented in the next chapter, is based on the set of pulsed I(V) measurement developed in this section. This dispersive model requires at least four dynamic I(V) datasets to identify its four model parameters accurately [1]. Therefore, in the next sections, independent
pulsed $I(V)$ measurements datasets corresponding to selected bias points under which surface trapping, buffer trapping and self-heating effects are separated.

### 5.3.1 Gate Trapping Dispersive Effect Characterization

As mention in the previous section, trapping effects in AlGaN/GaN HEMT are mainly related to the surface (gate) and buffer (deep or buffer) traps. These trapping effects should be characterized by pulsed $I(V)$ measurements at negligible device self-heating. Furthermore, the pulsed DC measurement should be taken from quiescent bias points where trapping effects are significant in order to determine fitting drain current parameters in the nonlinear drain current expression. Quiescent bias points that satisfy independent pulsed $I(V)$ measurement datasets should lie at low and high voltage ranges.

Surface state trapping effect is characterized by measuring pulsed $I(V)$ drain current at different quiescent bias points having different gate-source voltages but with constant drain-source voltage. This follows the assumption that the surface traps are mainly function of the gate-source bias voltage [12].

Therefore, surface trapping effects are characterized by pulsing from quiescent bias points having drain-source voltage fixed to zero ($V_{DS0} = 0V$); the dissipated power at this drain-source voltage bias points is negligible. The different quiescent bias points should have gate-source voltages spaced enough to see significant changes in the drain current due to the surface traps. Generally, the selection of the two bias gate-source voltages should be so that one is under pinch-off ($V_P$) and the other at the maximum gate-source voltage range.

For the 3.2-mm gate width AlGaN/GaN HEMT device, the gate-source pinch-off voltage $V_P$ is about -4.5V; therefore the two pulsed $I(V)$ measurements quiescent bias voltages for surface trapping characterization are selected as

$$V_{DS0} = 0V \quad (P_{diss} = 0); \quad V_{GS0} = -6V < V_P$$

$$V_{DS0} = 0V \quad (P_{diss} = 0); \quad V_{GS0} = 0V$$

Pulsed $I(V)$ measurement taken for the 3.2 mm AlGaN/GaN devices at this two bias points are shown in Figure 5.3. The pulsed measurements
have a pulse width of 1 µs or less and a repetition rate of 1 kHz (0.1% or less duty cycle). Self-heating is avoided during measurement process. The channel temperature of the device is determined by the selected quiescent bias point and the constant ambient temperature. A decrease in pulsed DC drain current is shown for measurements pulsed from bias point (-6V, 0V) as compared to pulsed from (0V, 0V) bias point; this clearly reflects the dispersive effect of the surface traps with knee voltage increase [3] [13] [14].

Figure 5.3 Pulsed I(V) measurements to characterize surface trapping of a 3.2-mm gate-width AlGaN/GaN HEMT on SiC with 0.5-µm gate-length. [Solid lines: Quiescent point (V_DS0 = 0V, V_GS0 = 0V); symbols: Quiescent point (V_DS0 = 0V, V_GS0 = -6V)].

5.3.2 Drain Trapping Dispersive Effect Characterization

Similarly, buffer (also drain or deep) trapping effect is characterized by measuring pulsed I(V) drain current at quiescent bias points having different drain-source voltages but with fixed gate-source voltage. This follows the assumption that the deep-level traps are mainly function of the drain-source bias voltage [12] [14].

Therefore, buffer trapping effects are characterized by pulsing from quiescent bias points having fixed gate-source voltage below pinch-off (V_GS0 < V_P). The dissipated power at these bias points is negligible. The
different quiescent bias points should have drain-source voltages spaced enough to see significant changes in the drain current due to the buffer trapping effect. Generally, the selection of the two bias drain-source voltages should be so that one is zero \((V_{DS0} = 0V)\) and the other at the maximum drain-source voltage range.

For the 3.2-mm gate-width AlGaN/GaN HEMT device, the fixed below pinch-off gate-source voltage is \((V_{GS0} = -6V)\). The two pulsed I(V) measurements quiescent bias voltages selected for drain trapping characterization are

\[
V_{GS0} = -6V \ (P_{diss} = 0); \quad V_{DS0} = 0V
\]

\[
V_{GS0} = -6V \ (P_{diss} = 0); \quad V_{DS0} = 54V
\]

Pulsed I(V) measurement taken for the 3.2-mm GaN devices at this two bias points are shown in Figure 5.4. Similarly, the measurements have been taken at constant ambient temperature. A decrease in pulsed I(V) drain current is shown for measurements pulsed from bias point \((54V, -6V)\) as compared to pulsed from \((0V, -6V)\) bias point. The measurements clearly reflect the dispersive effect of the buffer traps with considerable increase in the knee voltage [14].
Figure 5.4 Pulsed I(V) measurements to characterize buffer trapping of a 3.2-mm AlGaN/GaN HEMT HEMT. [Solid lines: Quiescent point ($V_{GS0} = -6V$, $V_{DS0} = 0V$); Symbols (squares): Quiescent point ($V_{GS0} = -6V$, $V_{DS0} = 54V$)].

5.3.3 Thermal Dispersive Effect Characterization

Pulsed I(V) measurements can be used in two ways to characterize self-heating dispersive effect and channel temperature in AlGaN/GaN HEMT devices nonlinear drain current. First, the channel self-heating could be modeled by including one new quiescent bias point for pulsed measurements in the active region. At this quiescent active bias point the HEMT device exhibits high power dissipation which generates high self-heating effect.

Using this approach, in order to acquire the necessary data, pulsed I(V) measurements have been performed at ($V_{GS0} = -2.7V$, $V_{DS0} = 40V$). As shown in Figure 5.5, a large self-heating effect is noticed when a pulsed I(V) measurement is taken at high power dissipation point (a class-AB bias point), as compared to the data taken at negligible power dissipation quiescent bias point ($V_{GS0} = 0V$, $V_{DS0} = 0V$).
This approach can be considered sufficient in case the model developed is for a specific class of operation and quiescent bias point, or for very narrow space region of operating quiescent bias points. Whereas, if the model is to be developed for CAD at arbitrary quiescent bias points, this approach looses accuracy as the bias point is shifted from the one developed for. Therefore, a more general and elaborate way to predict channel temperature should be used rather than this approach.

![Pulsed I(V) measurements to characterize the self-heating at high quiescent dissipate power in comparison with zero quiescent dissipated power.](image)

**Figure 5.5** Pulsed I(V) measurements to characterize the self-heating at high quiescent dissipate power in comparison with zero quiescent dissipated power. [Symbols: Quiescent point (V_{GS0} = 0V, V_{DS0} = 0V); solid lines: Quiescent point (V_{GS0} = -2.7V, V_{DS0} = 40V)].

The second proposed approach, that should give more accurate reflection of the channel temperature and hence evaluate correctly the thermal effect dispersive effect in the nonlinear drain current expression, is based on the HEMT channel temperature variation through chuck temperature controller. The thermal dispersive effect is characterized by measuring pulsed I(V) characteristics from a negligible power dissipation quiescent bias point (V_{GS0} = 0V, V_{DS0} = 0V) at different chuck temperatures. As shown in previous sections, at this quiescent bias point the trapping effects have negligible trapping effects. Therefore, the
dispersion resulting in the drain current will be directly related to the HEMT channel temperature difference controlled by the chuck temperature controller.

Using this approach, pulsed I(V) drain current measurements have been performed at bias quiescent point \((V_{GS0} = 0V, V_{DS0} = 0V)\) for distinct chuck temperature values. 20°C, 50°C, and 100°C curves are shown in Figure 5.6. A large decrease in drain current with an increase in the knee voltage is seen when pulsed I(V) measurements are taken at higher chuck temperatures as compared to measurements at low temperature. The dispersive effect in drain current due to thermal effect is related directly to the difference in HEMT channel temperature reflected by the thermo-chuck temperature difference.

It can be noticed clearly that both pulsed I(V) characterization approaches, presented above, show the same drain current behavior. Two

![Figure 5.6](image-url)
nonlinear drain current expressions based on these two approaches are investigated and implemented in the next chapter. A comparison is made in terms of thermal model implementation and extraction to propose relevant enhancement in model accuracy and validity region.

In the next section, another characterization technique is used to model the transient drain current. Transient pulsed measurements are used to determine the effect of surface trapping, buffer trapping, and self-heating on drain current. Obtained results will be implemented in the next chapter in the transient drain, gate, and thermal equivalent circuits.

### 5.4 Transients and Time Constants Characterization

In the previous section, the pulsed I(V) measurements were used to characterize the true dynamic RF dispersive effects in the nonlinear drain-source current expression. In this part a complementary characterization of the AlGaN/GaN HEMT device is operated under low-frequency excitations measurements. These excitations are responsible of quiescent bias point drain and gate voltages shifting, and therefore channel temperature variation. This fluctuation in bias point voltages affects the channel charge recombination (exchange) with surface (gate) and deep (drain) charges.

Therefore, in the next sections, drain current transient measurements will be presented in order to characterize this charge exchange due to low-frequency. Also, separated time constants are defined for both surface and buffer trapped charges through appropriate selection of quiescent bias points, it is important to accurately exclude other effects when characterizing one effect in resulting transient drain current.

Also, the channel temperature is subjected to variations under low-frequency variation in drain and gate voltages shifts due to change in power dissipation. Therefore, transient measurements at selected quiescent bias points are discussed for thermal time constant extraction.

The extracted three time constants are used in the next chapter in large-signal model implementation. RC equivalent circuit models will be added in the gate and the drain side to sense and model the low-frequency bias point voltage variation response due to trapping effects [1]. The trapping transient time constants define the time constant of the RC circuit. The values of the resistances are selected relatively large and the capacitances relatively small so that added trapping RC circuits affects only
transient trapping in the large-signal drain current model. Similarly, the thermal time constant is implemented in the RC equivalent thermal model.

5.4.1 Drain Transient and Time Constant Characterization

As described above, pulsed transient drain current measurement is used to obtain buffer trapping related time constant. This will be used to determine the elements of the drain side added RC circuit which describes the drain transient charge trapping. In order to obtain the drain transient trapping time constant, the thermal state of the device should be relatively unchanged at the quiescent bias and pulsed-to points. This may be accomplished in two different ways.

The first method to characterize the transient drain trapping constant is to select bias point and pulsed-to point along a curve of constant dissipated power [12]. Such drain current transient measurement results from a change in both the gate and drain voltages. Therefore, this characterization method shows clearly the transient trapping effect under constant dissipated power, but it leads to an overlapped gate and drain trapping effects characterization. Thus, separated drain and gate time constants cannot be determined. The method can be justified only if FET devices have one negligible transient effect [5].

The second method is to change only the drain voltage while keeping the gate voltage constant as proposed in reference [15]. In this case, the transient behavior shown in the drain current is dependent only on drain trapping charges. This can be done with the condition to have the bias point and the pulsed-to point power dissipations approximately unchanged (negligible power dissipation points). After the investigation of a large range of transient drain changed pulsed-to point, an overall characterization strategy of the drain time constant is determined as follows. After fixing the gate voltage at any arbitrary value above pinch-off and increasing the pulsed-to point drain voltage gradually, the general trend of the AlGaN/GaN transient measured drain current is found to be the same. At low values, at relatively negligible power dissipation points, the transient drain trapping is dominant, and the buffer time constant can be calculated using these results. As the drain pulsed-to point voltage is increased, the self-heating effect is shown to increase and affects the characterization of the transient drain trapping.
To summarize above statements, Figure 5.7 and Figure 5.8 are given as a sample to describe clearly the overall trend of the drain trapping charges transient for AlGaN/GaN HEMT studied in this work.

- **Buffer Transient from (-2V, 0V) to (-2V, 1V)**

  In Figure 5.7, the transient measurement from quiescent bias point (-2V, 0V) to the pulsed-to point (-2V, 1V) with negligible power dissipation is shown. It gives a drain current transient that increases from 550 mA to steady state current value of 571 mA. It is evident that the self-heating effect is negligible at this pulsed-to point due to negligible (zero) current level variation after reaching its steady state value. Therefore, since the gate voltage is kept constant, this drain current trapping transient characterizes completely the buffer charges transient effect. Consequently, Figure 5.7(a) shows the drain current transient trapping for a time interval of 1 ms. For buffer time constant extraction a time interval of 45 µs is shown in Figure 5.7(b). Using exponential curve fitting for these results we obtain buffer (drain) time constant $\tau_{DT}$ approximately equal to 1.3 µs, as shown in Figure 5.9(a).

- **Buffer Transient from (-0.5V, 0V) to (-0.5V, 3V)**

  Similar analysis is shown in Figure 5.8 for a high rating current pulsed-to point, the transient measurement from quiescent bias point (-0.5V, 0V) to the high dissipated power pulsed-to point (-0.5V, 3V). It gives a drain current transient that increases from 1704 mA to steady state current value of 1749 mA in an interval of approximately 20 µs, after which it starts to decrease. As shown in Figure 5.8(a), it is evident after this time interval (20 µs) that self-heating effect starts to dominate the drain current transient at this high rating current pulsed-to point (5.25W). Nevertheless, it is demonstrated from Figure 5.8(b) that the buffer trapping transient is showing the same trend and approximately the same time constant as in Figure 5.7(b) for negligible self-heating pulsed-to point. A set of measurements is done, and it is found that the fitting buffer time constant varies between 1 µs to 2 µs.
Figure 5.7 Buffer trapping time constant: Measured drain current transients for 3.2-mm AlGaN/GaN HEMT from bias points with fixed gate voltage with negligible power dissipation, (a) 1-ms time interval (b) 45-µs time interval [bias (-2V, 0V), pulsed-to (-2V, 1V)].
Figure 5.8 Buffer trapping time constant: Measured drain current transients for 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT from bias points with fixed gate voltage with higher rating current, (a) 1 ms range (b) 45 µs range [Bias (-0.5V, 0V), pulsed-to (-0.5V, 3V)].
Figure 5.9 Buffer trapping time constant from first-order exponential curve fitting parameters: (a) pulsed from bias point (-2V, 0V) to pulsed-to bias point (-2V, 1V) ($\tau_{DT} = 1.3 \, \mu s$) and (b) pulsed from (-0.5V, 0V) to pulsed-to bias (-0.5V, 3V) ($\tau_{DT} = 1 \, \mu s$).
5.4.2 Gate Transient and Time Constant Characterization

Similar procedure as in previous section is followed to characterize gate trapping transient. Pulsed transient drain current is measured to determine surface (gate) trapping time constant. It is used to determine the elements of the gate-side added RC circuit which describes the gate transient charge trapping. Also, in order to obtain the gate transient trapping time constant, the self-heating effect should be negligible at the quiescent bias and pulsed-to points. Furthermore, to characterize separately the gate transient trapping charges, the drain voltage should be kept fixed in both selected quiescent bias point and pulsed-to point at low rating current range. In this case, the transient behavior shown in the drain current is dependent only on surface gate trapping charges. Moreover, to excite the surface trapping charges the quiescent bias point gate voltage should be below pinch-off voltage, whereas the pulsed-to point gate voltage should be in the active region. In other words, the gate voltage should bring the AlGaN/GaN HEMT device from off-state to on-state [15].

The analysis of the results obtained for the surface transient charge trapping has shown a behavior similar to buffer transient charge trapping. After investigating the AlGaN/GaN HEMT devices for a large range of quiescent bias points and pulsed-to points, the characterization of surface time constant is achieved. First, the drain voltage is fixed at any arbitrary value above pinch-off, and then the gate voltage of the pulsed-to point is increased gradually. The general trend of the measured transient drain current is found to be the same as for the buffer tapping. At relatively negligible (low) power dissipation points, the transient gate trapping is dominant, and the surface time constant can be extracted directly from these results. As the pulsed-to point is shifted to high self-heating region, transient thermal effect is shown to become significant. To summarize this behavior, Figure 5.10 and Figure 5.11 are given as a sample to describe clearly the surface trapping time constant extraction for the 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT studied in this work.
Surface Transient from (-6V, 1V) to (-1V, 1V)

In Figure 5.10(a), the transient measurement from quiescent bias point (-6V, 1V) to the pulsed-to point (-1V, 1V) with negligible (low) power dissipation is shown. It is depicted that the surface trapping transient is dominant in the first time interval of 200 µs, after which the self-heating effect slowly starts to take place. In this time interval the drain current transient increases from 462 mA to initial steady state drain current value of 482 mA. Because the drain voltage is kept constant, this drain current transient characterizes only the surface trapping charges transient. Consequently, for surface time constant extraction a time interval of 200 µs is shown in Figure 5.10(b). By using exponential curve fitting of the presented results, surface (gate) time constant $\tau_{GT}$ of approximately 6 µs is obtained, as shown in Figure 5.12.

Surface Transient from (-6V, 3V) to (-2V, 3V)

As discussed previously, a sample of a high rating current pulsed-to point is used. The transient drain current measurement from quiescent bias point (-6V, 3V) to higher dissipated power pulsed-to point (-2V, 3V) is shown in Figure 5.11. It gives a drain current transient that increases from 560 mA to an initial steady state current value of 575 mA in an interval of approximately 100 µs, after which it starts to decrease. It has been noticed that self-heating effect starts to dominate the drain current transient earlier (after a smaller time interval) as high rating current pulsed-to point are selected. Nevertheless, the overall trend of the transient drain current related to surface trapping charges is kept the same for all investigated points. The surface trapping time constant $\tau_{GT}$ obtained in this case is approximately equal to 14.6 µs, as shown in Figure 5.13. A similar set of measurements is done, and it is found that the surface time constant varies between 6 µs to 14.6 µs.
Figure 5.10 Surface trapping time constant: Measured drain current transients from bias points with fixed drain voltage with low power dissipation, (a) 1-ms time interval (b) 200-µs time interval [Bias (-6V, 1V), pulsed-to (-1V, 1V)].
Figure 5.11 Surface trapping time constant: Measured drain current transient for bias points with fixed drain voltage with higher power dissipation point [Bias (-6V, 3V), pulsed-to (-2V, 3V)].

Figure 5.12 Surface trapping time constant extraction: Measured drain current transient for bias points with fixed drain voltage with low power dissipation. Solid line: First order exponential curve fit with $\tau_{GT} = 6$ $\mu$s; Symbols: Measured data [Bias (-6V, 1V), pulsed-to (-1V, 1V)].
Figure 5.13 Surface trapping time constant extraction: Measured drain current transient for bias points with fixed drain voltage with higher power dissipation point. Solid line: First order exponential curve fit with $\tau_{GT} = 14.6 \, \mu\text{s}$; Symbols: Measured data [Bias (-6V, 3V), pulsed-to (-2V, 3V)].

5.4.3 Thermal Transient and Time Constant Characterization

Similarly, as developed in Chapter 3, the thermal time constant can be extracted from drain current transient measurement at appropriate quiescent bias points. This characterization is useful in defining the equivalent RC equivalent circuit thermal model of the large-signal model. In case a first order RC thermal model is used, a single fitting exponential function of the measured drain current is needed. In case higher accuracy is requested, higher-order RC equivalent thermal model are investigated for model implementation; higher-order fitting exponential functions are used.

The drain current thermal transient characterization aims to define the time constant $\tau_{th}$ at which the AlGaN/GaN HEMT device reaches its new steady state channel temperature subjected to any instantaneous perturbation in power dissipation.

Therefore, pulsed I(V) drain current measurement from the quiescent bias point with negligible trapping should be used to characterize the HEMT thermal time constant(s). The pulsed-to point can be any point in the active region with high dissipated power within the device power safety limits. While measuring the transient drain current, it is preferable to fix pulsed-to gate voltage ($v_{GS}$), to exclude any gate trapping effect, while
changing the drain voltage successively to obtain dominant thermal transient state.

For 3.2-mm AlGaN/GaN HEMT device under investigation, as shown in Figure 5.14, increased self-heating is clearly seen with increasing pulsed-to drain voltage. When pulsed-to drain voltage reaches \( v_{DS} = 3V \), high rating current in 3.2-mm HEMT device, self-heating becomes dominant and the thermal time constant can be extracted from such transients.

![Figure 5.14](image)

**Figure 5.14** Thermal time constant characterization: Evolution of measured drain current transients \([\text{Bias point} \ (V_{GS0}, \ V_{DS0}) = (-1.5V, \ 0V) \ \text{pulsed-to point} \ (v_{GS}, \ v_{DS}) = (-1.5V, \ 1V : 7V)]\).

The drain current transient pulsed from bias point \( (V_{GS0}, \ V_{DS0}) = (-1V, \ 0V) \) pulsed-to a higher power dissipation bias point \( (v_{GS}, \ v_{DS}) = (-1V, \ 8V) \) is shown in Figure 5.15. A first order exponential curve fit of the transient drain current measured gives a thermal time constant of about 106.6 \( \mu \)s. As shown in the inset of Figure 5.15, the fast initial fall measurement data are not matching this first order low time constant curve fitting function. Therefore, a minimum of two distinct time constants should be considered to take this dynamic effect into account in drain current transient. This may be argued by the fast temperature increase in the thin epitaxial layer, and the slow temperature variation in SiC substrate due to layer thickness and high thermal conductivity.
Figure 5.15 Thermal time constant characterization: Transient drain current measurement (stars) and first order exponential function curve fit (solid line), bias ($V_{GS0}, V_{DS0}$) = (-1V, 0V) and pulsed-to ($v_{GS}, v_{DS}$) = (-1V, 8V). Inset for $0 < t < 200$ µs.

Multiple-time constants can be obtained by using higher-order exponential function curve fit. Figure 5.16(a) shows the curve fitting for this data curve up to the fifth order. It is apparent that as the order of the RC filter equivalent circuit model is increased, the simulated drain current matches better the measured thermal related transient drain current. For a better view of the fitting efficiency a comparison is shown in logarithmic scale in Figure 5.16(b). It is evident that the 1st order RC filter is not sufficient for accuracy requirements, whereas the 5th order RC implementation identifies to the transient measurements.
Figure 5.16 Thermal time constant characterization as function of the equivalent RC circuit order: (a) Linear time scale, (b) logarithmic time scale. Transient drain current measurement (symbols), and 1\textsuperscript{st}, 3\textsuperscript{rd} and 5\textsuperscript{th} order exponential function curve fit (solid lines) [Bias point (V\textsubscript{GS0}, V\textsubscript{DS0}) = (-1V, 0V) and pulsed-to point (V\textsubscript{GS}, V\textsubscript{DS}) = (-1V, 8V)].
A resume of thermal time constants is presented in Table 5.1, depending on the order of the exponential function required to fit the transient drain current. Therefore, the extracted thermal time constants of the HEMTs are used, as will be shown in the following sections, in the implementation of the RC thermal model through the calculation of the equivalent thermal capacitances.

<table>
<thead>
<tr>
<th>RC Order</th>
<th>$\tau_{th}$</th>
<th>$\tau_{th1} (\mu s)$</th>
<th>$\tau_{th2} (\mu s)$</th>
<th>$\tau_{th3} (\mu s)$</th>
<th>$\tau_{th4} (\mu s)$</th>
<th>$\tau_{th5} (\mu s)$</th>
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<td>Order 5</td>
<td>0.82022</td>
<td>5.8</td>
<td>83.4</td>
<td>41.1</td>
<td>1905.4</td>
<td></td>
</tr>
</tbody>
</table>

### 5.5 Thermal Resistance Characterization from Pulsed I(V)

In Chapter 3 the thermal model resistances were extracted through steady state thermal simulation. Here another alternative way to extract the thermal model equivalent resistances is presented. It is based on measurement characterization of the large-size AlGaN/GaN device. Therefore, to accurately estimate the channel temperature in the HEMT device, especially for devices with large gate-periphery, two reliable methods are presented here.

#### 5.5.1 Pulsed I(V) Isothermal Curves Overlapping

This method is based only on pulsed I(V) measurements. Pulsing is performed from two different quiescent bias points for different controlled chuck temperature values. The first pulsed I(V) curve is pulsed from the reference quiescent bias point ($V_{GS0} = 0V$, $V_{DS0} = 0V$) with zero power dissipation value ($P_{diss1} = 0$ W). Since pulsed I(V) current from this reference point delivers maximum drain current, the current level is reduced for comparison purpose, i.e. the controlled case temperature is set
to a higher value \((T_{\text{case1}} = 75^\circ \text{C})\). The second pulsed \(I(V)\) curve is operated from any arbitrary quiescent bias point in the active region \((V_{GS0}, V_{DS0})\) with known nonzero power dissipation value \((P_{\text{diss2}} = V_{DS0} \cdot I_{DS0})\). The controlled case temperature \((T_{\text{case2}})\) of the second curve is varied till the drain curve approximately overlaps the first curve obtained from reference bias point \((V_{GS0} = 0\text{V}, V_{DS0} = 0\text{V})\) [16].

As shown in Figure 5.17 for the 3.2-mm \((8 \times 400 \mu\text{m})\) AlGaN/GaN HEMT, the second pulse \(I(V)\) measurement quiescent bias point is \((V_{GS0} = -2\text{V}, V_{DS0} = -5\text{V})\) with \((I_{DS0} = 927.409 \text{mA})\) and power dissipation \((P_{\text{diss2}} = 4.637\text{W})\). The overlapping curves occur at case controlled temperatures of \((T_{\text{case1}} = 75^\circ \text{C})\) and \((T_{\text{case2}} = 10^\circ \text{C})\) for the reference and the active region bias points, respectively. At this point the thermal resistance can be obtained from the equations of the equivalent channel temperature as follows

1. Pulsed from \((0V, 0V)\): \(P_{\text{diss1}} = 0\text{W}\)

\[
T_{\text{ch}} = R_{\text{th}} \cdot P_{\text{diss1}} + T_{\text{case1}} = 75 \text{ C} \tag{5.1}
\]

2. Pulsed from \((-2V, 5V)\): \(P_{\text{diss2}} = 4.638\text{W}\)

\[
T_{\text{ch}} = R_{\text{th}} \cdot P_{\text{diss2}} + T_{\text{case2}} = R_{\text{th}} \cdot (4.638\text{W}) + 10^\circ \text{C} \tag{5.2}
\]

Since the two drain current curves overlap, the channel temperature should be equivalent to \((T_{\text{ch}} = 75^\circ \text{C})\). Hence, the resulting characterized total thermal resistance \(R_{\text{th}}\) is equal to \(R_{\text{th}} = 14^\circ \text{C/W}\).
Figure 5.17 Thermal resistance extraction from overlapped pulsed I(V) curves. Symbols: Pulsed I(V) measurement at case temperatures $T_{\text{case1}} = 75^\circ\text{C}$ for bias point $(V_{\text{GS0}}, V_{\text{DS0}}) = (0\text{V}, 0\text{V})$ with $P_{\text{diss1}} = 0\text{W}$; solid lines: Pulsed I(V) measurement at distinct case temperatures $T_{\text{case2}} = (75^\circ\text{C}, 40^\circ\text{C}, 10^\circ\text{C})$ for $(V_{\text{GS0}}, V_{\text{DS0}}) = (-2\text{V}, 5\text{V})$ with $P_{\text{diss2}} = 4.638\text{W}$. All curves are for $v_{\text{GS}} = -2\text{ V}$.

5.5.2 Pulsed I(V) and Static DC Curves Crossing

Here, the thermal resistance is extracted from two drain current measurements curves for two different bias points with distinct case temperatures. The intersection point of the two measured drain current curves is the point at which the equivalent channel temperature is the same; the drain current delivered is the same [11]. The equivalent channel temperature will be described for both curves as

$$T_{\text{ch}} = R_{\text{th}} \cdot P_{\text{diss1}} + T_{\text{case1}} \quad (5.3)$$

$$T_{\text{ch}} = R_{\text{th}} \cdot P_{\text{diss2}} + T_{\text{case2}} \quad (5.4)$$

where $P_{\text{diss1}}$ and $P_{\text{diss2}}$ are the dissipated power at bias point 1 and bias point 2 under controlled case temperature $T_{\text{case1}}$ and $T_{\text{case2}}$, respectively. By
equating the two expressions, the resulting thermal resistance can be extracted to be equal to

\[ R_{th} = \frac{\Delta T_{\text{case}}}{\Delta P_{\text{diss}}} \]  \hspace{1cm} (5.5)

To obtain this intersection, the first selected drain curve is based on pulsed \( I(V) \) measurements from quiescent bias point \( (V_{GS0} = 0 V, V_{DS0} = 0 V) \) to a pulsed-to curve points \( (V_{GS}, V_{DS}) \). At this bias point the dissipated power is zero and the temperature is equal to the temperature of the case \( (T_{\text{case1}} = 100^\circ C) \). The temperature of the case is varied till the intersection happens with a second curve obtained under static DC measurement. The channel temperature will be given by the expression

\[ T_{\text{ch}} = R_{th} \cdot P_{\text{diss1}} + T_{\text{case1}} = T_{\text{case1}} \]  \hspace{1cm} (5.6)

At the intersection point of the two curves, the power dissipation of the second curve is directly related to the product of the static DC drain voltage and drain current value \( (P_{\text{dissQ}} = I_{DSQ} \cdot V_{DSQ}) \). With the temperature of the case equal to ambient temperature \( (T_{\text{amb}} = 20^\circ C) \), the equivalent channel temperature will be given by

\[ T_{\text{ch}} = R_{th} \cdot P_{\text{dissQ}} + T_{\text{amb}} \]  \hspace{1cm} (5.7)

from which the thermal resistance can be found to be equal to

\[ R_{th} = \frac{T_{\text{case1}} - T_{\text{amb}}}{P_{\text{dissQ}}} \]  \hspace{1cm} (5.8)

As shown in Figure 5.18, for the 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT device under consideration, the pulse \( I(V) \) measurement pulsed-to curve is selected for pulsed-to gate voltage curve \( (V_{GS} = -1V) \), also the static DC curve is for \( (V_{GSQ} = -1V) \). The intersection point is \( (I_{DSQ}, V_{DSQ}) = (1.41A, 4.27V) \) at a power dissipation of 6.02W \( (P_{\text{dissQ}} = I_{DSQ} \cdot V_{DSQ}) \). The obtained total thermal resistance is shown to be equal to \( R_{th} = 13.28^\circ C/W \) .
Figure 5.18 Thermal resistance extraction at the intersection point \((V_{GSQ}, V_{DSQ}) = (-1V, 4.27V)\) at drain current \(I_{DSQ} = 1.41A\) and power dissipation \(P_{dissQ} = 6.02W\). Pulsed I(V) measurement at case temperature \((T_{case1} = 100°C)\) for \(V_{GS} = -1V\), the static DC curve at case temperature \((T_{amb} = 20°C)\) for \(V_{GSQ} = -1V\).

As shown, using both thermal resistance extraction methods above, the difference in thermal resistance value is within 5%. It is estimated that even though the pulsed I(V) measurements technique is used to reduce the self-heating effect, always a small residual heating is present. Therefore, the thermal resistance should be greater than or equal to the highest extracted value \(R_{th} = 14 °C/W\).

For the sake of completeness, a third method can be used for thermal resistance extraction for devices with no trapping effect. This method cannot be used for our AlGaN/GaN HEMT device due to the large surface trapping. It is based on the measurements of three gate current curves. Two pulsed measurements of the gate current versus gate voltage variations are from zero power dissipation bias point \((V_{GS0}, V_{DS0}) = (0V, 0V)\) for two different temperatures \((T_1, T_2)\). The third pulsed measurement curve is selected at a known non-zero power dissipation bias point \((P_{diss0})\) at the temperature \((T_1)\). For a fixed gate current level \(I_{gs0}\), as shown in Figure 5.19, the three corresponding gate voltages are obtained. The resulting thermal resistance is given by [11]
Figure 5.19 Thermal resistance extraction from pulsed I(V) measurements for fixed-gate current at two different quiescent bias points with two different case temperatures.

5.6 Thermal Model From Pulsed I(V) Characterization

At this point all the necessary characterization measurements and parameters are covered. From the time constants defined in Table 5.1 and the total thermal resistance obtained in the previous section, an equivalent RC circuit thermal model implementation up to the 5th order is possible for accurate static and dynamic channel temperature prediction, as presented in Figure 3.1. First, the distinct equivalent thermal model resistances are extracted from their corresponding drain current transient, as shown in Table 5.2. Then, the equivalent thermal capacitances are evaluated from individual time constants from the expression \( \tau_{thi} = R_{thi} C_{thi} \), as it is illustrated in Table 5.3.

The extracted high-order thermal model data and the drain (buffer) and gate (surface) time constants are directly integrated within the nonlinear part of the electrothermal large-signal model equivalent circuit in CAD, as will be shown in the next chapter. Using these measurements
correlated trapping and self-heating sub-circuits, a net increase in the accuracy of the model and in the convergence enhancement in both input power range and speed will be established.

**Table 5.2** Thermal resistances for 3.2-mm AlGaN/GaN HEMTs on SiC.

<table>
<thead>
<tr>
<th>RC Order</th>
<th>$R_{th}$ ($^\circ$C/W)</th>
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<th>$R_{th2}$</th>
<th>$R_{th3}$</th>
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<td>1.6</td>
<td>1.3</td>
<td>2.8</td>
<td>0.5</td>
<td>7.8</td>
</tr>
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**Table 5.3** Thermal capacitances for 3.2-mm AlGaN/GaN HEMTs on SiC.

<table>
<thead>
<tr>
<th>RC Order</th>
<th>$C_{th}$ ($\mu$F)</th>
<th>$C_{th1}$</th>
<th>$C_{th2}$</th>
<th>$C_{th3}$</th>
<th>$C_{th4}$</th>
<th>$C_{th5}$</th>
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**References**


Chapter 6

Electrothermal Large-Signal Modeling and Verification for AlGaN/GaN HEMTs

After electrical and thermal small-signal and large-signal characterization of the AlGaN/GaN HEMT device has been discussed in the previous chapters, all necessary parameters and functions needed for large-signal electrothermal equivalent circuit implementation in CAD are determined. Its parameters are totally constructed from relevant electrical and thermal characterization.

Therefore, in this chapter, the extraction, implementation and verification of the large-signal table-based equivalent circuit model are treated. First, the nonlinear drain-source current, gate-source current, gate-drain current, and charge sources are detailed. These are based on trapping and self-heating pulsed I(V) characterization described in Chapter 5 and bias dependent small-signal S-parameters (capacitances) obtained in Chapter 4. Also, they are function of instantaneous and average gate and drain voltages and estimated channel temperature. The drain-source current models the channel conduction current, whereas the charge sources derivatives model the displacement currents. Equivalent sub-circuits are used to capture trapping and self-heating transient circuits: This representation uses data from trapping and self-heating time constants and thermal resistance characterization presented in Chapter 5. Second, the implementation of the model into CAD environment is discussed. ADS software table-based large equivalent circuit model is constructed using symbolically defined devices (SDD). Finally, distinct validation tests are presented for linear and efficient RF high power amplifiers applications to modern wireless communication basestation.
6.1 Large-Signal Equivalent Circuit Model Extraction

The large-signal equivalent circuit used to model the intrinsic part of AlGaN/GaN HEMT is shown in Figure 6.1. Nonlinear charge sources and gate currents parameters of this model are derived from the distributed small-signal model described in Chapter 4 to preserve consistency between small and large-signal models [1].

Figure 6.1 Intrinsic large-signal model topology for AlGaN/GaN HEMT including characterized higher-order self-heating sub-circuit (3rd order shown) and characterized buffer and surface trapping sub-circuits.
This model takes into account a non-quasi static implementation and includes all dispersion effects in the drain current implementation. Two quasi-static gate current sources $I_{gs}$ and $I_{gd}$ are used in the equivalent circuit model to describe the gate conduction currents. Similarly, two quasi-static gate charge sources $Q_{gs}$ and $Q_{gd}$ are used to describe the gate displacement currents [1]. Two bias-dependent charging resistances $R_i$ and $R_{gd}$ are implemented in series with $Q_{gs}$ and $Q_{gd}$, respectively, to model the nonquasi-static effect in the channel. The charging time constants for the depletion region capacitances in the channel are described by resulting time constants of the products $R_iC_{gs}$ and $R_{gd}C_{gd}$. This implementation improves high frequency model simulations.

The dispersive non-quasi static drain current model $I_{ds}$ is implemented to account for trapping and self-heating effects. The drain current is obtained through the evaluation of the applied intrinsic voltages $V_{gs}$ and $V_{ds}$. The induced current dispersion due to trapping and dynamic self-heating is controlled by the RF components of these intrinsic voltages [1].

The gate (surface) trapping and drain (buffer or deep) trapping time constants $\tau_{GT}$ and $\tau_{DT}$, respectively, are modeled using a first order RC high-pass circuit at the gate and drain sides respectively. Resistances $R_{GT}$ and $R_{DT}$ in series with $C_{GT}$ and $C_{DT}$, respectively, are used to model the small dispersive leakage currents in the gate and drain paths. The capacitors values $C_{GT}$ and $C_{DT}$ are chosen in the order of 1 pF to model the small stored charges in the surface and buffer traps [2]. These charges are primarily related to the leakage currents from the gate metal edge to the surface or from the channel into the buffer layer [3]. The values of $R_{GT}$, $R_{DT}$, $C_{GT}$, and $C_{DT}$ are selected so that the time constants $R_{GT}C_{GT}$ and $R_{DT}C_{DT}$ products are equal to the trapping time constants $\tau_{GT}$ and $\tau_{DT}$ obtained through the trapping characterization of the AlGaN/GaN HEMT device in Chapter 5. In the case of lack of characterization means, approximate trapping time constants in the order of $10^{-5}$ to $10^{-4}$ s can be used with series resistances in the order of 1 MΩ [2]. This trapping implementation improves model accuracy for describing low frequency dispersion channel transconductance and output conductance, which is related mainly to the surface and buffer traps [4].

Furthermore, the drain current implementation accounts for the static and dynamic self-heating dispersion effect through the thermal equivalent circuit model presented in Figure 6.1. The channel temperature of the AlGaN/GaN HEMT transistor is obtained from the thermal model through
the calculation of the instantaneous power dissipation. This instantaneous channel equivalent temperature of the AlGaN/GaN HEMT transistor is embedded in the drain current model to correct induced thermal dispersion effect. For static DC drain current, the static channel temperature rise $\Delta T$ can be obtained with the product of the channel dissipated power to the device thermal resistance. A first-order or higher low-pass filter equivalent circuit is included to determine the estimated channel temperature due to the static and quasi-static (dynamic) dissipated powers. The values of the thermal capacitances $C_{thi}$ and thermal resistances $R_{thi}$ in the thermal model are selected from the thermal resistances and thermal time constants obtained in thermal simulations and/or device characterization in Chapter 3 and Chapter 5. In case of a single order low-pass filter thermal model implementation is used, a large thermal time constant is selected in the millisecond range (2 ms) [1] [2].

6.1.1 Drain Current Modeling

To derive accurate drain current model for devices which exhibit significant trapping and self-heating dispersive effects, it is not possible to use conventional CW S-parameters measurements techniques [5] [6]. These measurement techniques are consistent for low power FET devices modeling with negligible self-heating effects. As self-heating increases with larger power densities, nonlinear large-signal model parameters become highly dependent on average and instantaneous voltages as well as the channel temperature. Therefore, to model nonlinear drain current for power AlGaN/GaN HEMT devices, with technology immature problems (passivation, substrate), pulsed DC measurements under appropriate quiescent bias conditions have to be used. By introducing pulsed I(V) measurements in large-signal current modeling [7], the developed large-signal model started to give RF output power simulations comparable to measurement. Furthermore, the extraction of the time constants of the different dispersion effects, discussed in previous chapter, is a key factor in large signal modeling accuracy; they predict the DC to RF frequency transition.

In the next sections, procedures are discussed that describe the derivation of I(V) functions of the large-signal model from pulsed DC measurements and dispersive effects time constants extracted in the previous chapter.
6.1.1.1 Dispersive Table-Based Drain Current Model

An accurate dispersive drain current model (which accounts for trapping and self-heating effects) can be derived from a set of pulsed I(V) measurements taken at appropriate quiescent bias conditions. The drain current model can be expressed as [1]

\[ I_{ds}(V_{ds}, V_{gs}, V_{dso}, V_{gso}, P_{diss}) = I_{ds,iso}^{DC}(V_{gs}, V_{ds}) + \alpha_G(V_{gs}, V_{ds}) (V_{gs} - V_{gso}) + \alpha_D(V_{gs}, V_{ds}) (V_{ds} - V_{dso}) + \alpha_T(V_{gs}, V_{ds}) P_{diss} \]  

(6.1)

where \( I_{ds,iso}^{DC} \) is the isothermal DC with zero self-heating effect. \( \alpha_G \) and \( \alpha_D \) model the dispersion effects due to the surface trapping and buffer trapping effects, respectively. \( \alpha_T \) gives the dispersion effect due to the self-heating effect. The amount of trapping induced current dispersion depends on the rate of dynamic change of the applied intrinsic voltages \( V_{gs} \) and \( V_{ds} \) with respect to their average values of \( V_{gso} \) and \( V_{dso} \). Therefore, the current dispersion is mainly stimulated with the RF components of the gate-source and drain-source voltages [as described by \( (V_{gs} - V_{gso}) \) and \( (V_{ds} - V_{dso}) \) in (6.1)].

The self-heating induced dispersion is caused by both static and dynamic components of the drain current (dominated by low frequency components). Therefore, \( P_{diss} \) in (6.1) accounts for the static and quasi-static intrinsic power dissipation. The drain current model has four unknowns \( I_{ds,iso}^{DC}, \alpha_G, \alpha_D \) and \( \alpha_T \). To determine these unknowns, there should be at least a set of four input data. The data should be acquired from a pulsed I(V) characteristics at suitable quiescent bias conditions that leads to four independent linear equations.

A further enhancement in the nonlinear drain current expression in (6.1) can be elaborated with the available simulation and characterization data. The expression in (6.1) is suitable in case that less data are available, mainly lack of thermal characterization and thermal time constants of the AlGaN/GaN HEMT devices [1]. As presented in previous sections, these difficulties have been bypassed by an effort in both thermal simulations (Chapter 3) and device characterization (thermal resistance, thermal time constant, and trapping time constants in Chapter 5). Therefore, the drain
current model can be expressed in a more general I(V) model [8] and can be written as

\[
I_{ds}(V_{gs}, V_{ds}, V_{gs0}, V_{ds0}, T_{ch}) = I_{ds0} \cdot f_{\text{trapD}} \cdot f_{\text{trapG}} \cdot f_{\text{thermal}} \tag{6.2}
\]

where \(V_{gs}\) and \(V_{ds}\) are the instantaneous applied intrinsic voltages. \(V_{gs0}\) and \(V_{ds0}\) are the DC components which are dependent on the quiescent bias voltages and the mean values of gate and drain terminal intrinsic voltages. The channel temperature \(T_{ch}\) models the influence of thermal effects.

The reference current \(I_{ds0} = f(V_{gs}, V_{ds})\) is a function of the instantaneous terminal voltages only [9]. It is the pulsed I(V) drain current measurements from reference quiescent bias \((V_{gs0} = 0V, V_{ds0} = 0V)\). For a given pulsed-to-intrinsic voltage point \((V_{gs}, V_{ds})\), the pulsed DC drain currents from this reference bias point are larger than any other bias point. This I(V) characteristics is considered as dispersion-free, which means that it is free of current collapse and it has minimum knee voltages. Consequently, the I(V) characteristics represents the greatest potential of the device under RF operation.

The drain trap function \(f_{\text{trapD}} = f(V_{ds0}, V_{gs}, V_{ds})\) is due to varying drain bias voltages. It can be identified by taking pulsed DC measurements with varying drain bias voltages but at a fixed gate bias voltage. Similarly, \(f_{\text{trapG}} = f(V_{gs0}, V_{gs}, V_{ds})\) is used to model traps due to gate bias variations. It can be determined by taking pulsed DC measurements with varying gate bias voltages but at a fixed drain bias voltage. The parameter \(f_{\text{thermal}} = f(P_{\text{diss}}, T_{ch})\) models channel current variation due to channel power dissipation and temperature.

To identify the parameters \(f_{\text{trapD}}, f_{\text{trapG}}, f_{T}\) in (6.2) a large series of measurements is needed [8]. Therefore, a linearized approximation of (6.2) with respect to a nominal bias point \((V_{gs0}, V_{ds0})\) and channel temperature \(T_{ch}\), which requires less number of pulsed DC measurements, is proposed for AlGaN/GaN HEMT devices. The linearization, adopted in the present work, is a variant of (6.1), it is described using extrinsic voltages as [10]
\[ I_{DS}(V_{GS}, V_{DS}, V_{GS0}, V_{DS0}, T_{ch}) = I_{DS,iso}^{DC}(V_{GS}, V_{DS}) + f_G(V_{GS}, V_{DS}) \left[ V_{GS} - V_{GS0} \right] + f_D(V_{GS}, V_{DS}) \left[ V_{DS} - V_{DS0} \right] + f_T(V_{GS}, V_{DS}) \left[ R_{th} (P_0 - P_0^*) + (T_{ch} - T_{ch}^*) \right] \] (6.3)

where, \( I_{DS,iso}^{DC}(V_{GS}, V_{DS}) \) is an ideal isothermal DC characteristic corresponding to a reference channel temperature \( T_{ch}^* \). The functions \( f_G \) and \( f_D \) model the deviation between the static and dynamic drain current due to gate and drain traps, respectively. The thermal effect function \( f_T \) accounts for the device self-heating power dissipation (\( P_0 \)) and case temperature (\( T_{ch} \)) variations.

The thermal resistance \( R_{th} \) is the total thermal resistance between channel and case (chuck for devices on wafer), a detailed extraction procedure is discussed in Chapter 3 and Chapter 5 using both simulations and characterization, respectively. The change in the channel temperature is presented by the self-heating effect (\( R_{th} (P_0 - P_0^*) \)) and the change in case temperature (\( T_{ch} - T_{ch}^* \)).

The identification of the four model parameters \( I_{DS,iso}^{DC}(V_{GS}, V_{DS}) \), \( f_G(V_{GS}, V_{DS}) \), \( f_D(V_{GS}, V_{DS}) \) and \( f_T(V_{GS}, V_{DS}) \) requires a minimum of four pulsed DC datasets taken from different quiescent bias and/or ambient temperature conditions of the FET. They are obtained by solving simultaneously the four corresponding linear equations.

One more important feature of this implementation is that I(V) model may be obtained for constant or varying case ambient temperatures. Also, the integration of higher-order thermal model is possible for more accurate RF output power prediction. If the model parameters are to be identified for a fixed case temperature with a first order low-pass circuit thermal model then an explicit knowledge of the thermal resistance of the device structure is not necessary. This may be reduced to the drain current expression in (6.1) [2]. In this case, the drain current expression in (6.3) can be reduced to drain current expression in (6.1), by rewriting the thermal coefficient expression in (6.3) as \( \alpha_T(V_{GS}, V_{DS}) = f_T(V_{GS}, V_{DS}) \cdot R_{th} \).
6.1.1.2 Drain Current Model Fitting Coefficients Extraction

The characterization of the AlGaN/GaN HEMT, handled in the previous chapter, has provided the necessary pulsed IV measurement input data needed to determine the different coefficients in the nonlinear drain current equation in (6.3). Solving the system of linear independent equations, constituted by the drain current measurement data at these selected set of bias points shown in Figure 5.3 to Figure 5.6 of the previous chapter, the bias dependent nonlinear drain current fitting parameters $I_{ds,iso}^{DC}$, $f_G$, $f_D$ and $f_T$ are obtained.

Figure 6.2 shows the four extracted dispersive effects fitting parameters as a function of intrinsic bias voltages $(V_{gs0}, V_{ds0})$. It shows smooth curves and a clear transition from pinch-off region to active regions. All parameters are zero in pinch-off region and at zero drain voltage as expected.

The isothermal drain current $I_{ds,iso}^{DC}$, as shown in Figure 6.2, increases as the drain voltage and/or the gate voltage increases. The buffer trapping coefficient $f_D$ increases near the knee voltages, but decreases for higher drain voltage. This happens due to negative (strong decrease) or positive (weak decrease) pulsed-to drain voltage $V_{ds}$ relative to quiescent bias drain voltage $V_{ds0}$, as discussed in Chapter 5. The surface trapping parameter $f_G$ has a sharp decrease when $V_{gs}$ increases, as shown in Figure 6.2. Similar behavior is obtained for thermal dispersive coefficient $f_T$, it follows the usual trend of AlGaN/GaN HEMT devices. It increases with an increase in the drain current and voltage.
Figure 6.2 Extracted bias-dependent dispersive drain current model fitting parameters: (a) isothermal drain current $I_{DS,iso}^{DC}(v_{GS},v_{DS})$, (b) buffer trapping parameter $f_D(v_{GS},v_{DS})$, (c) surface trapping parameter $f_G(v_{GS},v_{DS})$ and (d) thermal parameter $f_T(v_{GS},v_{DS})$.

6.1.2 Nonlinear Charge Sources Modeling

One of the important key factors in enhancing intermodulation distortion prediction in AlGaN/GaN HEMT large-signal modeling procedure is the determination of the nonlinear gate charge sources [11]. Furthermore, the resulting large-signal model has to reproduce the small-signal measured data accurately. This is known as model consistency. Therefore, to achieve consistency between the bias-dependent small signal model intrinsic capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$ and the large-signal model nonlinear charge sources $Q_{gs}$ and $Q_{gd}$ a special formulation should be used [12]. These charge sources are obtained through the integration over the small signal capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$ as given in expressions as follows [2] [13].
where \((V_{go}, V_{do})\) is an arbitrary integration starting point.

The resulting surfaces of \(Q_{gs}\) and \(Q_{gd}\) as a function of the intrinsic gate and drain voltages \(V_{gs}\) and \(V_{ds}\) are shown in Figure 6.3 for the 3.2-mm gate-width AlGaN/GaN HEMT device on SiC substrate considered in this work. As expected, the shapes obtained are similar to the reported ones reported in [14] [2]. This reflects the suitability of the extraction procedure for the device under investigation. Furthermore, the determined values of \(Q_{gs}\) and \(Q_{gd}\), which are in orthogonal set of intrinsic \(V_{gs}\) and \(V_{ds}\), are written in CITI-file format for ADS implementation in the large-signal model part as look-up tables accessed through Data Access Components (DACs).

![Figure 6.3](image_url)

**Figure 6.3** Calculated gate charge sources (a) \(Q_{gs}\) and (b) \(Q_{gd}\) versus intrinsic voltages for a 3.2-mm (8x400 µm) gate width AlGaN/GaN HEMT with 0.5 µm gate length on SiC substrate.

**6.1.3 Nonlinear Gate Current Modeling**

The gate currents \(I_{gs}\) and \(I_{gd}\) can be determined in two distinct methods. The first is based on an integration formulation of the intrinsic gate conductances \(G_{gsf}\) and \(G_{gdf}\) obtained in the small-signal modeling procedure presented in Chapter 4, assuming that \(G_{gsf}\) is gate-source voltage dependent only. They can be calculated by integrating the intrinsic gate conductances \(G_{gsf}\) and \(G_{gdf}\) as [2]
\[
I_{gs}(V_{gs}, V_{ds}) = I_{gs}(V_{gs0}, V_{ds0}) + \frac{V_{gs}}{V_{gs0}} \int G_{gsf}(V, V_{ds0}) dV
\]  
(6.5a)

\[
I_{gd}(V_{gs}, V_{ds}) = I_{gd}(V_{gs0}, V_{ds0}) + \frac{V_{gs}}{V_{gs0}} \int G_{gdf}(V, V_{ds0}) dV - \frac{V_{ds}}{V_{ds0}} \int G_{gdf}(V_{gs0}, V) dV
\]  
(6.5b)

This first approach is easier to implement compared to the second approach based on experimental pulsed DC measurements setup [2]. It is based on direct extraction of the gate-forward and gate-to-drain breakdown currents from pulsed DC measurements. The gate-forward current in the large-signal model of the power HEMT devices can be measured with high accuracy and safety under pulsed DC measurement set-up based on Diva-D265. Similar results have shown increased accuracy in large-signal modeling based on pulsed DC measurements [15] [16].

Gate-forward current measurements for different size AlGaN/GaN HEMTs on SiC substrates have shown its dependency on both gate- and drain-voltages [15]. This proves the deficiency in using the usual diode equation model of a Schottky contact, such a model would be correct for zero drain or source to drain voltages. This behavior of HEMT gate-forward current should be reflected in large-signal modeling.

In implementing these nonlinear current sources in ADS, either an analytical function of two variables to fit these data or a table-based component can be used. Figure 6.4 shows a sample of extracted gate-drain and gate-source currents. In this work, obtained \( I_{gs} \) and \( I_{gd} \) are written in a CITI-file format to be accessed in ADS® as a look-up table through Data Access Components (DAC).

![Image](image-url)

**Figure 6.4** Extracted nonlinear gate current sources as function of intrinsic drain and gate voltages for a 3.2-mm AlGaN/GaN HEMT, (a) \( I_{gs} \) and (b) \( I_{gd} \).
6.2 Large-Signal Model Implementation in CAD

After the extraction of the extrinsic parameters in the previous chapter and the nonlinear large-signal parameters as described in previous sections, all electrical parameters of the large-signal model of the high power AlGaN/GaN HEMT device are available to construct the large signal model described in Figure 6.5.

The large-signal model in Figure 6.5 is implemented in Agilent’s Advanced Design System, ADS® as it is shown in Figure 6.6. The extracted optimized extrinsic parameters, described in Chapter 4, are single valued parameters and can be presented by lumped elements. Therefore, as described in details in Chapter 4, the extrinsic bias-independent elements $C_{pga}$, $C_{pda}$, $C_{gda}$, $L_g$, $L_d$, $L_s$, $C_{pgi}$, $C_{pdi}$, $C_{gdi}$, $R_g$, $R_d$, and $R_s$ are represented by lumped passive elements (see Figure 6.6).

The $RC$ lumped elements circuits on the gate side ($R_{GT}C_{GT}$) and drain side ($R_{DT}C_{DT}$) side define the gate and the drain charge trapping time constants respectively. These time constants are obtained from pulsed DC transient measurements characterization of the AlGaN/GaN HEMT device as discussed in Chapter 5. Similarly, the thermal model equivalent circuit is represented by 5$^{th}$ order $RC$ filter lumped elements sub-circuit; values are extracted from thermal modeling as discussed in Chapter 3 and Chapter 5. In Figure 6.6(a), a 5$^{th}$ order RC filter extracted in Chapter 5 is implemented.

The extracted nonlinear intrinsic bias-dependant model parameters $Q_{gs}$, $I_{gs}$, $Q_{gd}$, $I_{gd}$, $R_{gd}$, $R_i$, and $\tau$ are written in look-up table elements versus $V_{gs}$ and $V_{ds}$ as index variables in an output file. These nonlinear model parameters are function of an orthogonal set of intrinsic voltages ($V_{gs}$, $V_{ds}$). Similarly, the fitting bias-dependent nonlinear parameters $f_G$, $f_D$, and $f_T$ of the drain current are also written in look-up tables versus the orthogonal set of $V_{gs}$ and $V_{ds}$ in an output file. They are implemented in one of the standard file format read by ADS®, like CITI-file format.
Figure 6.5 Electrothermal large-signal model for 3.2-mm gate width device size, (a) complete electrothermal model, (b) intrinsic large-signal model and (c) 3rd order sub-circuit thermal model representation.
During simulation process in ADS®, these look-up tables (data files) are accessed using multi-purpose Data Access Components (DACs) file reader. Furthermore, the reading, interpolation, and extrapolation of the parameters from the data files relies on DAC selected options. Figure 6.6(b) shows a sample of DAC used for drain current nonlinear parameters data file handling, the interpolation and extrapolation options have to be specified. In Figure 6.6(a), the implementation of the table-based large signal nonlinear model is based on Symbolically Defined Device (SDD) feature in ADS®. It is an equation-based element that enables us to define nonlinear components without using source codes. Any correlation between its port voltages, port currents, and/or their derivatives can be defined.

A 10-port SDD, as shown in the center of Figure 6.6(a), is used to implement the nonlinear intrinsic part of the HEMT device. Port 1 through 5 correspond to \((Q_{gs}, I_{gs}), (Q_{gd}, I_{gd}), R_i, R_{gd}\) and \(I_{ds}\), respectively. The instantaneous power is calculated at port 6, from which the equivalent channel temperature variation is determined by the voltage at port 9 through the thermal model RC network representation. This temperature variation is used to estimate the thermal dispersive effect in the drain equation. Port 7 and 9 are used to evaluate the high frequency components of the gate and drain voltage, \((V_{gs} - V_{gs0})\) and \((V_{ds} - V_{ds0})\). Finally, the transconductance time delay is modeled with a delayed gate voltage at port 10, it is obtained by the expression \(V_{10} = V_1 e^{-j\omega r}\) through the 1Ω port termination and the weighting function \(H[4] = e^{-j\omega r}\).
Figure 6.6 Implementation of the large-signal GaN HEMT model in ADS® software: (a) large-signal extrinsic lumped elements and intrinsic symbolically defined device (SDD) implementation including the 5th order thermal sub-circuit. (b) Sample of data access component (DAC).
6.3 Large-Signal Model Simulation and Verification

To testify the validity and reliability of the large-size large-signal AlGaN/GaN HEMT devices modeling procedure, developed in our department and extended by this work, a series of distinct test and verification measurements should be fulfilled by model implemented in Figure 6.6. The model verification should include small-signal as well as large-signal power levels under different bias conditions. The table-based large-signal model is verified through S-parameters, pulsed I(V), large-signal single-tone and finally large-signal two-tone simulations versus measurements. Other model verification tests may be used too, such as complex modulated signal (W-CDMA), depending on the purpose for which the model is developed. All data considered in the next sections are for large-size AlGaN/GaN HEMT device on SiC substrate with 3.2-mm (8x400 µm) gate width and 0.5-µm gate length on wafer.

6.3.1 Model S-Parameter Verification

First verification is the consistency of the large-signal model. Therefore, the large-signal model simulations should be verified to fulfill the S-parameters and pulsed-IV measurements from which it has been derived. S-parameter simulations compared with measurements are presented at distinct bias points at different power dissipations in Figure 6.7 to Figure 6.9 for the large-signal dispersive model. It is shown that the large-signal model has reproduced the small-signal behavior of the device. This agreement between simulation and measurement verifies large-signal model consistency with extracted small-signal model.

The simulated small-signal gain $S_{21}$ matches completely the measurements for all selected bias points, this reflects the reliability of the enhanced drain current extraction and implementation procedure. As the simulated gain $S_{21}$ is directly related to the extracted large-signal electrothermal drain current through pulsed I(V) characterization and not CW S-parameters. Similarly, the same accuracy is noticed in the simulated input-reflection coefficient $S_{11}$ and the reverse transmission coefficient $S_{12}$ with measurements. This accuracy verifies the consistency of the gate nonlinear parameter extraction procedure, these being dependent on S-parameter measurements. Concerning the output-reflection coefficient $S_{22}$, a small deviation is noted in the simulated results as compared to measurement at high power bias points, while the model simulation
describes accurately its response versus frequency, as shown in Figure 6.8 and Figure 6.9. This small discrepancy is a usual issue in output reflection coefficient $S_{22}$ in large-signal modeling; it is mainly due to measurements limited data base and uncertainties [15] [2] [17].

**Figure 6.7** Large-signal model S-parameter verification of 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT at deep class-AB point ($V_{GS0} = -3.4V$, $V_{DS0} = 45V$, $I_{DS0} = 25 mA$), (simulation: solid line, measurement (circles)).

**Figure 6.8** Large-signal model S-parameter verification of 3.2-mm (8 x 400 µm) AlGaN/GaN HEMT at active class-AB point ($V_{GS0} = -2.4V$, $V_{DS0} = 45V$), (simulation: solid line, measurement (circles)).
6.3.2 Pulsed I(V) Verification

As described in the previous section, the second consistency validation test of the large-signal model is the pulsed I(V). Therefore, the large-signal model simulations should be verified to fulfill the pulsed-IV measurements at different quiescent bias conditions than those used in drain current fitting parameters extraction. These simulations should sustain convergence behavior of the model in digital and transient related communications applications.

The comparison of the pulsed DC simulation and measurement data are presented for different classes of operations and bias points in pinch-off and active region. All results have shown good agreement and are well consistent with measurement as described in Figure 6.10. This confirms the model robustness in predicting bias-dependency of the dispersive trapping and self-heating effects.
Figure 6.10 Pulsed I(V) verification: (Solid lines) model simulation, (dashed lines) measurements, and (dots) model implementation as in [2] for pulsed-to gate voltage range of ($V_{GS} = -3.3V$ to 0.3V: step 0.6V) at different quiescent points. [(a) ($V_{DS0} = 45V$, $V_{GS0} = -3.1V$) and (b) ($V_{DS0} = 30V$, $V_{GS0} = -2V$).]
6.3.3 Large-Signal Single-Tone Verification

Another model verification test for high power amplifiers applications is the large-signal single-tone (CW) input power sweep. This gives the capability to predict the device output power response for fundamental tone and higher harmonics. This measures the reliability of the large-signal model nonlinear elements extraction procedure; on which higher orders harmonics output power are dependent. It reflects directly the discrepancy between simulation and measurement in the 1dB compression point in large-signal operation of HPAs.

In this regard, a single-tone verification test sample is shown in Figure 6.11 for a class-AB bias point ($V_{GS0} = -2.7\, \text{V}$, $V_{DS0} = 45\, \text{V}$, $I_{DS0} = 300\, \text{mA}$). The developed electrothermal large-signal model brings a net improvement in the output power characteristics validation test as compared to previous implementation in [2]. This supports that the trapping and self-heating effects, being the source of nonlinearities in HEMT devices, have been captured accurately by this enhanced modeling procedure. A very good agreement between simulations and measurements for large-signal fundamental output power is made evident through the more accurate prediction of the 1dB compression point. The small difference that may still be sensed is mostly related to the current rating and power limit in pulsed I(V) measurements database (2A limit under DiVA setup) and the error introduced in drain current data extrapolation at high pulsed-to points.

Also, this comparison has shown a good agreement for the fundamental power gain and efficiency for a wider input power sweep. The model also shows good prediction for higher harmonic components of the output power. This enhanced implementation has shown increased simulation convergence behavior and wider range of input power sweep due to realistic large-signal model trapping and self-heating elements extraction procedure, as described in the previous chapter.
Figure 6.11 Single-tone power sweep simulations (lines) and measurements (symbols) at class-AB bias point ($V_{GS0} = -2.7\,\text{V}$, $V_{DS0} = 45\,\text{V}$, $I_{DS0} = 300\,\text{mA}$) at 2.14 GHz with a 50Ω source and load termination: (a) fundamental tone output power, (b) 2\textsuperscript{nd} harmonic output power, (c) 3\textsuperscript{rd} harmonic output power, (d) fundamental output power, gain and power added efficiency.
6.3.4 Two-Tone Intermodulation Distortion Prediction

The nonlinearity prediction capability is one of the major goals of this work. This enhanced dispersive large-signal model development procedure should show clear and evident higher performance as previously followed procedure [2]. The nonlinearities of the AlGaN/GaN HEMTs large-signal model is commonly tested using a two-tone simulation. It is typically the most used method for the linearity analysis of devices and amplifiers, because it describes the behavior of the device under real modulated large-signal conditions.

Two-tone test signals are used in order to determine intermodulation distortion (IMD) product terms from the device nonlinearities. This intermodulation distortion depicts the nonlinear model elements and their higher-order derivatives accuracy. Two-tone large-signal measurements setup is performed with calibration procedure as described in [18] and [19]. A two-tone signal with center frequency of 2.14 GHz and carrier spacing of 200 kHz has been used. It represents a non-constant envelope signal with peak-to-average power ratio of 6 dB (or peak-to-average voltage ratio of 3 dB). Detailed comparison between measured and simulated fundamental output power, gain, efficiency, estimated channel temperature, and IMD3 terms are shown in Figure 6.12, Figure 6.14, and Figure 6.15 for different bias points. The large-signal model simulation results show a very good agreement with the measured data.

To show the effect of the introduced enhancements in the large-signal characterization and modeling procedure on intermodulation prediction and accuracy, simulation results are compared between the previous implementation as detailed in [2] and the proposed procedure in this work in Figure 6.13 and Figure 6.16. It is shown that the proposed investigations and model implementation have led to more accurate results due to the enhanced (trapping and self-heating) electrothermal drain current implementation. The prediction of the fundamentals output power, gain, and third order intermodulation distortion terms (IMD3) are improved significantly even at low power range where the previous model implementation lacks accuracy, as presented in Figure 6.16. Moreover, the enhanced model CAD implementation converges faster in simulations and achieves higher input power sweep than the previous model implementation. This is due to the more realistic trapping and self-heating sub-circuits representation in the large-signal model equivalent circuit. These sub-circuits extraction procedures are detailed in Chapter 3 and Chapter 5.
Figure 6.12 Two-tone signal response for class-AB operation conditions ($V_{GS0} = -2.7V$, $V_{DS0} = 40V$, $I_{DS0} = 300$ mA) with $f_0 = 2.14$ GHz and $\Delta f = 200$ kHz in a $50\Omega$ source and load environment: (a) Fundamental output power and (b) gain; measurement (symbols) and simulation (lines).
Figure 6.13 Two-tone signal response comparison between results obtained by: (a) Procedure presented in this work and (b) previous procedure as described in [2]. Measurement (symbols) and simulation (lines) for ($V_{GS0} = -2.7\, \text{V}$, $V_{DS0} = 40\, \text{V}$, $I_{DS0} = 300\, \text{mA}$) with $f_0 = 2.14\, \text{GHz}$ and $\Delta f = 200\, \text{kHz}$ in a $50\, \Omega$ environment.
Figure 6.14 Two-tone signal response for class-AB operation conditions ($V_{GS0} = -3\text{V}$, $V_{DS0} = 45\text{V}$, $I_{DS0} = 190 \text{ mA}$) with $f_0 = 2.14 \text{ GHz}$ and $\Delta f = 200 \text{ kHz}$ in a $50\Omega$ source and load environment. (a) Fundamental output power, (b) gain, and (c) IMD3 output power; (Simulation: line, measurement: symbols).
Figure 6.15 Two-tone signal response for deep class-AB operation conditions (\(V_{\text{GS0}} = -3.475\text{V}, V_{\text{DS0}} = 40\text{V}, I_{\text{DS0}} = 25\text{ mA}\)) with \(f_0 = 2.14\text{ GHz}\) and \(\Delta f = 200\text{ kHz}\) in a 50Ω source and load environment: (a) Variation in channel temperature estimation (\(\Delta T_{\text{ch}}\)), (b) fundamental output power, (c) gain, and (d) IMD3 output power; (Simulation: line, measurement: symbols).
Figure 6.16 A 3.2-mm AlGaN/GaN HEMT two-tone signal response comparison between measurement and simulation obtained by: (a) Enhanced procedure presented in this work and (b) previous procedure in [2] for (\(V_{GS0} = -3.475V\), \(V_{DS0} = 40V\), \(I_{DS0} = 25\) mA \(\approx 10\%\) of \(I_{DSS}\)) with \(f_0 = 2.14\) GHz and \(\Delta f = 200\) kHz in a 50\(\Omega\) environment; (Simulation: line, measurement: symbols).

References


Chapter 7

Conclusion and Further Work

7.1 Conclusion

With the increase in RF output power density, reaching more than 41 W/mm, large-signal modeling turns out to be critical due to increased parasitics, high trapping dispersion and self-heating effects present in large-size devices. Also, the reduced large-signal measurement database, such as costly measurement equipments are needed for high current ratings characterization (more than 2A), increases nonlinear electrothermal large-signal model extraction difficulty and deteriorates total model accuracy. These problems arise mainly in simulating intermodulation distortions and higher-order harmonics. For the large-signal modeling strategy developed previously in our department the discrepancy appears for large-size devices far from the region of focus, whereas for other’s works they are very common in modeling relatively small device sizes.

Therefore, in this work the large-signal modeling strategy, which was initially developed in our department for low and medium power GaAs and GaN devices, has been extended to large-size high power GaN HEMTs. It models accurately large-signal nonlinearities and enables distortion prediction even for regions close to pinch-off and linear-region. Hence, due to the importance of intermodulation distortions and higher-order harmonics nonlinearities prediction in HPAs, large-signal model response has been enhanced in this regard. The AlGaN/GaN HEMT device nonlinearity sources have been deeply investigated; precisely, surface trapping, buffer trapping and self heating nonlinearities and their effects on HEMT nonlinear drain current have been accurately characterized.
The AlGaN/GaN HEMT structure thermal profile was first investigated to have a deep insight of the heat transfer and heat dissipation mechanisms in the layered structure. The analysis revealed key advantages of using this approach. It has shown to be flexible to any large-signal model topology; the equivalent thermal model extraction technique could be easily associated to the nonlinear electrothermal large-signal model extraction procedure. For topologies where thermal measurement characterization fails to give an equivalent thermal model, the proposed thermal simulation procedure intervenes successfully. As an example, for distributed multi-finger HEMT structure, the unit cell electrical model can be obtained from the modeling of a single or double finger structure, whereas for the equivalent thermal sub-circuit is not possible due to its non-uniform channel temperature distribution in total HEMT structure. To estimate the correct channel temperature in this implementation topology, each unit cell is associated with its proper thermal model elements (thermal resistance and capacitance).

The small-signal model implementation in this modeling strategy is based on the robust method previously developed in our department. The parasitic capacitances are very critical for the extraction of the extrinsic elements and the whole extraction procedure. A careful analysis is carried out for cold pinch-off and cold forward S-parameter measurement database and upper frequency limit under which extraction is possible, for which the small-signal intrinsic model elements are frequency independent. Simulations and verification tests have been performed and the small-signal extraction procedure has revealed its accuracy and robustness for large-size devices.

Based on optimized extrinsic small-signal parameters, HEMT large-signal intrinsic bias dependent passive elements, nonlinear charge sources, and currents are extracted in a bottom-up modeling approach to preserve model consistency. Nonlinear charge sources being a consistent part in nonlinearity prediction in large-size large-signal modeling are satisfying path-independent integration. The obtained extrinsic passive elements are represented as lumped elements in ADS® environment and the table-based intrinsic elements are implemented in look-up tables accessed through data access components (DACs).

To enhance large-signal model nonlinearity prediction, distortion sources have been analyzed and integrated in their relevant large-signal model equivalent circuit elements. First, investigation has been
concentrated on dispersive effects. Gate trapping, drain trapping and self-heating dispersion effects characterization have been handled under large signal operation, from which nonlinear electrothermal large-signal uncorrelated drain current fitting parameters were extracted. Each dispersion effect related fitting parameter is characterized by isolating the other two dispersion effects. Second, table-based isothermal drain current is extracted for zero trapping and neglected self-heating conditions. This isothermal table-based extraction is operated under pulsed I(V) measurement with a thermo-chuck temperature controlled measurement setup. The four fitting functions have been written in DACs look-up tables in ADS® environment as a function of the intrinsic terminal voltages.

Enhanced formulation has been carried out in the transformation of voltages from extrinsic terminals to intrinsic terminals to reduce the introduced numerical processing error, mainly in the linear and knee region. The large-signal nonlinear drain current implementation has been modified to enable the developed large-signal model to operate under any ambient temperatures and instantly respond to any temperature fluctuations due to RF signal dynamics.

Furthermore, to increase model nonlinearity accuracy and prediction capability for RF signal dynamics, HEMT transient characterization has been elaborated, and corresponding extracted parameters has been included in the large-signal model. First, trapping transients were investigated deeply under different transient bias conditions measurements. The surface trapping time constant and the drain trapping time constants have been determined separately and accurately for the large-size HEMT device under investigation with negligible self-heating condition. Moreover, thermal transients also have been characterized to account for RF signal dynamics effect on HEMT channel temperature. Higher-order time constant is derived from measurement in parallel with the thermal resistance characterization and extraction using distinct measurement techniques. This total thermal resistance has been determined from chuck controlled temperature based pulsed I(V) measurement setup.

Using enhanced RC equivalent sub-circuit implementation, the device characterization related trapping time constants have been represented on the gate and drain sides to sense and contribute in transient response of nonlinear output drain current. Furthermore, multi-time constant RC equivalent sub-circuit has been implemented to evaluate the instantaneous equivalent channel temperature response under DC and RF signal
excitation. The equivalent RC filters sub-circuits elements have been extracted from the pulsed I(V) transient measurements through curve fitting routines implemented in Matlab programming language up to the 5th order. For thermal sub-circuit, the total thermal resistance of the structure must be constrained to the sum of the higher order RC sub-circuit resistances. This calculated instantaneous channel temperature value is recursively updated in simulation process with the nonlinear drain current.

The electrothermal large-signal nonlinear drain current fitting functions and large-signal intrinsic elements have been implemented in ADS® around a symbolically defined device (SDD). The fitting function and the nonlinear charge sources and currents are accessed from the look-up tables through DACs. A very good agreement between simulations and measurements for large-signal fundamental output power is made evident through accurate prediction of the 1dB compression point. The small difference that may still be sensed is mostly related to the current rating and power limit in pulsed I(V) measurements database (2A limit under DiVA setup) and its corresponding error introduced in drain current transformation and extrapolation at high pulsed-to points. The implemented realistic measurement characterization based values RC filters sub-circuits have increased model accuracy to intermodulation distortions and higher order harmonics. This supports that the trapping and self-heating effects, being the source of nonlinearities in HEMT devices, have been captured accurately in this enhanced modeling procedure. Moreover, convergence is assured for higher simulated input power range with less time complexity. Previously estimated values did not physically reflect the real trapping and thermal transient effect, and hence electrical and thermal memory effects on total drain current nonlinearities.

7.2 Further Work

Besides the achievements of the electrothermal large-size large-signal model presented in this work, many other related research issues can be proposed for further improvements. Some interesting future research investigations can be oriented to the following directions.

- The thermal modeling procedure proposed can be extended to the study of the power AlGaN/GaN HEMT device thermal management. Different semiconductor layers such as solder layer, heat-sink layer and package-type can be modeled and thermal models can be
extracted and implemented in CAD environment prior to realization. This issue is essential for AlGaN/GaN HEMT power bar device thermal analysis, design, modeling and simulation. This type of transistor chip is reaching hundreds of watts per single unit and therefore needs a considerable effort regarding thermal management techniques.

- The extraction software programs developed is based on Comsol-Matlab programming environment. Through the association of these two environments, a complete and flexible multi-physics programming facility is offered. Physics-based electrothermal modeling procedure could be proposed as an extension and as a complementary option for HEMT device investigation in regards with physical parameters and structure topology. This can be handled provided that technology related HEMT physical parameters are available; unfortunately it was not the case for us during the time interval of this work.

- Large-size large-signal model scaling is a very promising extension of the presented electrothermal modeling procedure. The large-size large-signal can be extracted for a unity cell AlGaN/GaN HEMT composed of a single-finger or double-finger configuration and extended to inter-digitated multi-finger structure. The equivalent circuit thermal model extraction is directly determined for individual fingers through developed simulation procedure while the parasitic elements are extracted by scaling rules for electrical model.

- Thermal time constant and trapping time constant variation with temperature can be investigated for more robust large-size large-signal electrothermal modeling procedure. This extension of the work needs a stable power AlGaN/GaN HEMT device technology. The temperature dependent time constants can be implemented in ADS environment. It can be associated directly to the instantaneous channel temperature determined by the high-order thermal model.

- Higher-order time constants equivalent circuit topology can be used for transient surface and buffer trapping in the large-signal model at the drain and gate sides. A more elaborate and efficient circuit configuration implementation in ADS environment is possible to meet this extension. Also, it is necessary to have stable AlGaN/GaN HEMT device technology to be operated under transient measurement with different chuck-temperature controlled setup.
Measurement data processing needs to be enhanced more to reduce numerical processing error introduced in the interpolation and extrapolation of the dispersive nonlinear drain current extraction. The routines for external terminal voltages transformation to intrinsic voltages should be improved for accurate large-signal model; for example series resistances variation with power dissipation level and channel temperature can be introduced.
The rapid growth in high data rate communication systems has introduced new high spectral efficient modulation techniques such as LTE-A (long term evolution-advanced) for 4G (4th generation) systems. These techniques have provided a broader bandwidth but introduced high peak-to-average power ratio (PAR) at the high power amplifier (HPA) level of the base transceiver station (BTS). To avoid spectral spreading due to high PAR, rigorous requirement on linearity is needed which brings the HPA to operate at large back-off power at the expense of power efficiency. Consequently, high power devices are fundamental in HPAs for high linearity and efficiency. Recent wide bandgap devices, in particular AlGaN/GaN HEMT, have offered higher power level with superior linearity-efficiency trade-off in microwaves communication.

For cost-effective HPA design to production cycle, accurate computer aided design (CAD) AlGaN/GaN HEMT models are essential to reflect real response with increasing power level and channel temperature. Therefore, large-size AlGaN/GaN HEMT large-signal electrothermal modeling procedure has been proposed. The HEMT structure analysis, characterization, data processing, model extraction and model implementation phases have been covered in this thesis including trapping and self-heating dispersion accounting for nonlinear drain current collapse. The verification of the resulting table-based large-size large-signal electrothermal model implementation has illustrated high accuracy in terms of output power, gain, efficiency and nonlinearity prediction with respect to standard large-signal test signals.